Innovations in Large-Area Electronics Conference (innoLAE) 2016

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SPEAKER PROGRAMME

February 2016

1–2

Robinson College, Cambridge
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Day 1	InnoLAE 2016	
09:30-10:00	Keynote 1 **Professor Donal Bradley, University of Oxford** *Plastic electronics: electrode materials, injection layers and solution processed small molecule OLEDs*	
10:30-12:30	Session 1: Integrated smart systems, devices and circuits **1.1 Invited speaker: Dr Martina Pintani, Cambridge Display Technology** *Solution processed electronic devices at CDT: overview of technology platforms and current performance* **1.2 Dr Vincenzo Pecunia, University of Cambridge** *Solution-based hybrid organic/metal-oxide integration for complementary circuits on foil* **1.3 Dr Simon Ogier, NeuDrive** *0.5MHz 5 stage ring oscillator circuits and low cost customization technologies for organic logic devices* **1.4 Dr Xiaojun Guo, Shanghai Jiao Tong University** *Printable organic transistor technology platform for expanding "More than Moore"*	Session 2: Manufacturing technologies 1 **2.1 Rob Hendriks, NovaCentrix** *Ultra-fast fabrication of printed electronics through photonic curing and soldering* **2. 2 Dr Tom Harvey, CPI** *Roll-to-roll digital photolithography* **2.3 Guy Bex, Holst Centre** *Photonic processes in printed electronics (Printing with Light)* **2.4 Dr Sebastian Wood, National Physical Laboratory** *Towards the in-line inspection of organic photovoltaic cells using surface-function correlation*
14:00-16:00	Session 3: Energy harvesting and storage **3.1 Invited speaker: Prof. Henry Snaith, University of Oxford** *Title TBD* **3.2 Dr Jenny Baker, SPECIFIC** *Printing of graphene nanoplatelets as low cost electro-catalysts for dye sensitised solar cells* **3.3 Dr Youmna Mouhamad, University of Swansea** *Mass volume printing of energy harvesting device: development of antenna and tunable capacitor system* **3.4 Dr Pritesh Hiralal, University of Cambridge** *Powering the internet of things: screen printed batteries*	Session 4: Emerging materials for organic electronics **4.1 Harry Cronin, DZP Technologies** *Novel low-cost conductive layers for printed electronics* **4.2 Dr Iyad Nasrallah, University of Cambridge** *Towards highly stable polymer electronics* **4.3 Dr Sheida Faraji, University of Manchester** *Solution-processed high-k nanocomposite gate dielectrics for use in low-voltage field-effect transistors (OFETs): Studying the influence of surface functionalisation of nanoparticles* **4.4 Dr Emre Polat, University of Glasgow** *Synthesis of large area graphene for high performance in flexible optoelectronic devices*
16:30-17:00	Keynote 2 **Prof. Antonio Facchetti, Polyera Corporation** *Materials synthesis and process engineering for organic and hybrid opto-electronics*	
17:00-18:10	Session 5: New market opportunities and technology trends (plenary) **5.1 Invited speaker: Dr Tung-Huei Ke, IMEC** *Thin-film integrated circuits for IoT and sensor systems* **5.2 Invited speaker: Dr Guillaume Chansin, IDTechEx** *Printed and flexible electronics in wearables and sensors*	

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Day 2	InnoLAE 2016	
09:00-09:55	Keynote 3 **Dr Faiz Sherman, Procter & Gamble** *Do sensors have a place in consumer packaged goods*	
10:20-12:20	Session 6: Internet of Things and sensors **6.1 Invited speaker: Prof. Harri Kopola, VTT** *Technologies towards Digital Paradise* **6.2 Dr Tiziano Agostinelli, FlexEnable** *Activating surfaces: Flexible electronics for large-area Sensors* **6.3 Dr Ehsan Danesh, University of Manchester** *Fully solution-processed OFET platform for vapour sensing applications* **6.4 Dr Michael Renn, Optomec** *Aerosol jet printing of antenna and sensors for IoT*	Session 7: Bio-electronics for smart wearable and implantable medical devices **7.1 Invited speaker: Prof. Magnus Berggren, Linköping University** *Organic bioelectronics- new tools for medicine and biology* **7.2 Invited speaker: Prof. Stephanie Lacour, EPFL** *Soft bioelectronics for robotics and neuroprosthetics* **7.3 Invited speaker: Dr Roy Katso, GlaxoSmithKline** *The opportunities of bioelectronics medicines as a treatment paradigm* **7.4 Prof. Matti Mäntysalo, Tampere University of Technology** *Printed epidermal electronics*
13:30-16:00	Session 8: Manufacturing technologies 2 **8.1 Invited speaker: Prof Rhodri Williams, Swansea University** *Advanced rheology for printing large area electronics* **8.2 Dr Dana Borsa, Meyer Burger** *Manipulation and control of spatial ALD layers for flexible devices* **8.3 Dr Dimitra Georgiadou, Imperial College London** *Assessing the scalability of adhesion lithography towards highly efficient co-planar nanogap rectifying diodes* **8.4 Dr David Bird, CPI** *Production and measurement of roll-to-roll ALD barriers for electronic applications; results from FP7 projects R2R-CIGS and NanoMend* **8.5 Dr Daniel O'Connor, National Physical Laboratory** *Implementation of a linear optical encoder for high precision in line position referencing of plastic film in a roll-to-roll system*	Workshop: Lasers for additive and subtractive LAE manufacturing **W.1 Prof. Ioanna Zergioti, National Technical University of Athens** *Laser direct writing of large area electronics on flexible Substrates* **W.2 Dr Emeric Biver, Oxford Lasers** *Recent advances in laser processes to print electrical connections: towards industrialization* **W. 3 Dr Adam Brunton, M-Solv** *Laser and inkjet tools for large area electronics Manufacturing* **W. 4 Dr Demosthenes Koutsogeorgis, Nottingham Trent University** *Laser annealing of indium gallium zinc oxide: A platform towards flexible and large area processing of thin film transistors* **W.5 Panel discussion** **Moderator: Prof. Bill O'Neill, Institute for Manufacturing, Department of Engineering, University of Cambridge** *Laser microfabrication in flexible electronics: what opportunities and how to scale up for mass market applications*

Plastic Electronics: Electrode Materials, Injection Layers and Solution Processed Small Molecule OLEDs

Professor Donal D.C. Bradley

Departments of Engineering Science and Physics, University of Oxford, Division of Mathematical, Physical and Life Sciences, 9 Parks Road, Oxford OX1 3PD

Abstract

This paper will report work undertaken to address a number of current topics in plastic electronics, namely the development of (i) electrode material alternatives to Indium Tin Oxide for flexible substrate devices, (ii) novel interlayer materials that promote injection and extraction of charges and (iii) solution processed OLEDs using small molecule emitters including phosphorescent and thermally activated delayed fluorescence materials.

Biography

Professor Donal D.C. Bradley CBE, FRS, CEng, FIET, FInstP, FRSA is Head of the Mathematical, Physical and Life Sciences Division and Professor of Engineering Science and Physics at the University of Oxford.

As Head of Division, Professor Bradley has overall responsibility for science and engineering, addressing both strategic and operational aspects of the delivery of education, research and impact, and ensuring an environment that supports excellence in scientific research.

In addition, he leads a research programme within the Departments of Engineering Science and Physics. His research focuses on the physics and application of novel materials and devices, especially the use of solution processed semiconductors for energy efficient displays and lighting, solar energy, sensing, imaging and communications. He is a co-inventor of conjugated polymer electroluminescence, an innovation that launched the wider field of plastic electronics.

Professor Bradley was elected a Fellow of the Royal Society in 2004, of the Institute of Physics in 2005 and of the Institution of Engineering and Technology in 2013. He was awarded a CBE in 2010 for services to science.

SESSION 1:

Integrated smart systems, devices and circuits

Invited Speaker

Solution processed electronic devices at CDT: overview of technology platforms and current performance

Dr Martina Pintani

Cambridge Display Technology Limited, Unit 3 Cardinal Park, Cardinal Way, Godmanchester, PE29 2XN

Abstract

At CDT we believe that the way to advance the field of printable electronics relies on focusing on key components such as flexible displays, lighting, photovoltaic devices, photodetectors and transistor circuits. To further the development, we have at our disposal in-house a variety of solution-based materials and can employ a number of printing methods. This allows for greater flexibility in the design, improved functionality, enhanced form factor and scaling of electronic systems to larger areas. In this presentation we will show recent progress at CDT in devices and materials for these areas. In particular we will discuss:

Development in Printed Transistors, which we have used to develop key circuit elements such as amplifiers and logic gates, as well as more standard display backplane applications. These components are crucial to realise an integrated all-printed system platform, such as needed to amplify the output signal of printed organic photodetectors.

Printable Organic Photodetectors (OPDs) which CDT can process to large area devices using non-halogenated solvents and that have been shown to give enhanced device efficiency. OPDs can be employed in medical and industrial applications ranging from image detectors to low resolution sensor devices.

Progress in solid state lighting, where devices fabricated on plastic and using solutions compatible with R2R processing have been demonstrated to achieve high lm/W values at good CCT and CRI. These devices incorporated a scattering technology developed at CDT that enables efficient light extraction from plastic devices.

Advances in Flexible OLEDs, where CDT has recently reported high efficiencies and very low drive voltage. The devices have also been shown to have very good mechanical stability and a shelf-life of more than 2 years achieved via a simple lamination process for encapsulation (no evaporated layer required for encapsulation), and they are fabricated with tools compatible with R2R processing. These specifications and their cost proposition make these air-processed flexible devices an ideal solution for a new generation of OE application like wearables.

Biography

Martina Pintani completed a Master's degree in Physics at the University of Trento (Italy) in 2003, followed by a PhD at Imperial College London under the supervision of Prof. Donal D.C. Bradley's. She then joined Cambridge Display Technology (CDT) in 2007 where for a number of years she worked on OLED materials development and on improving the understanding of OLED degradation mechanisms. She is now working as Senior Scientist within the Flexible OLED team at CDT, looking at characterising and improving performance and understanding of air-processed OLED devices fabricated in-house on flexible substrates.

(1.2) Solution-Based Hybrid Organic/Metal-Oxide Integration for Complementary Circuits on Foil

Vincenzo Pecunia* and Henning Sirringhaus

Cavendish Laboratory, University of Cambridge, Cambridge, CB3 0HE, United Kingdom

In recent years, hybrid circuit integration comprising organic and metal-oxide active materials has emerged as a new paradigm for complementary large-area electronics. On one hand, semiconducting polymers have surpassed the performance and stability of amorphous silicon as p-type materials; on the other, amorphous-metal-oxide semiconductors have been shown to possess excellent n-type semiconducting properties. It has been thus envisioned that the solution-based integration of semiconductors of these two classes can deliver complementary circuits for potentially low-cost large-area electronics.

Here we present our work on complementary hybrid circuits on flexible substrates. Our integration relies on a high-performance p-type polymer and an n-type binary oxide as active materials. Both semiconductors are used in combination with a polymer gate dielectric, which ensures a high degree of flexibility of the overall transistor stack and resulting circuits. All electronic materials are processed from solution and at low temperature, allowing integration on a plastic substrate. We employed our technology to fabricate transistor circuits, which constitute the first example of hybrid solution-based functional integration on foil.

Keywords
organic semiconductors, metal-oxide semiconductors, hybrid integration, complementary circuits, flexible electronics.

Biography
Dr Vincenzo Pecunia is a Research Associate at the Optoelectronics Group of the Cavendish Laboratory, University of Cambridge. His research interests include charge transport in organic and metal-oxide semiconductors, solution-based organic, metal-oxide and hybrid transistors, and process integration for flexible and printed electronics. Vincenzo joined the EPSRC Centre in May 2014 to work on the iPESS project.

Vincenzo carried out his doctoral work on organic electronics under the supervision of Professor Henning Sirringhaus at the University of Cambridge. Before his PhD, he completed his BSc and MSc in Electronics Engineering at Politecnico di Milano, Italy.

(1.3) 0.5MHz 5 stage ring oscillator circuits and low cost customization technologies for organic logic devices

Simon Ogier[1], Mike Simms[1], Mohammad Mashayekhi[2], Jordi Carrabina[2], Lluís Terés[3]

[1] NeuDrive Ltd. Biohub, Alderley Park, Macclesfield, UK, [2]Universitat Autònoma de Barcelona, Spain, [3]IMB-CNM (CSIC), Barcelona, Spain.

Keywords: OTFT, FlexOS, Circuits, Gate Array, ASIC

Organic transistor technology has improved over recent years and FlexOS™ organic semiconductors currently achieve charge mobility levels of >4cm^2/Vs in short channel (<10 micron) devices over large substrate sizes. NeuDrive is developing the materials and process technology for generating arrays of devices for flexible displays, logic and sensor devices using established large area manufacturing techniques. The low temperature processes used coupled with the inherent flexibility of organic TFT devices are seen as important for new product concepts with sufficient durability and a cost competitive fabrication process.

This presentation describes the approach taken to generate logic devices using a 5 mask process with minimum feature size of 5 microns. 5 stage ring oscillators were measured with operating frequencies of greater than 0.5MHz at operating voltages of 40V (see figure 1). Stage delay for the fastest oscillators were calculated at ~160ns. Inverter configurations that produced slower oscillators (f=150kHz) were functional down to 20V operating voltage and it is expected that this could be reduced further through gate dielectric engineering to improve on the relatively low capacitance of these devices (6nFcm^{-2}).

Gate arrays were constructed so that layer 5 of the masking process could be used to customize the logic circuits through the wiring design of a single metal layer. Whilst the density of transistors is lower in a gate array, this approach allows designers to realise circuits quickly and with a significantly reduced mask cost. Basic cells of the gate array can be individual TFTs or logic gates (NOT, NAND2, NAND3 etc). Approaches to wire the cells using digital methods (such as ink-jet) will also be presented, demonstrating how a custom circuit could be built without the need to incur any mask redesign costs at all.

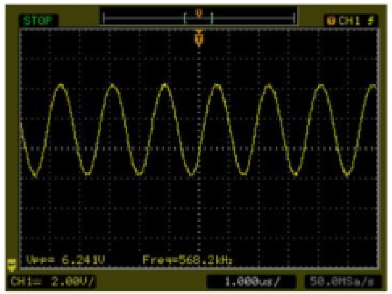

Figure 1 – Oscilloscope trace of 5 stage FlexOS™ ring oscillator operating at 40V supply (note: the voltage swing is 1.8X the displayed value due to the mismatch between the picoprobe impedance and oscilloscope input impedance)

Biography

Dr Simon Ogier graduated in Physics with Electronics and Instrumentation from Leeds University in 1996 and completed a PhD researching Molecular ion channels as novel biosensors in 2000. Since that time he has worked in the field of organic electronics, developing high performance organic semiconductors for flexible and low temperature transistor applications. Since joining NeuDrive as CTO in 2015 he has been working to integrate FlexOS™ materials into display pilot manufacturing lines in addition to exploring the potential of the technology for flexible displays, logic and sensor devices.

(1.4) Printable Organic Transistor Technology Platform for Expanding "More than Moore"

Xiaojun Guo

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E-mail: x.guo@sjtu.edu.cn

Keywords: organic transistor, printed electronics, low voltage, hybrid integration

Abstract

The rapid progress of silicon microelectronics is meeting both physical and economic limits of technology scaling. With popularity of Internet of Things and the Trillion Sensors Universe, more diverse applications with features of being large area, flexible/conformable, disposable, and fast production are demanded, which are difficult for silicon microelectronics. On the other hand, with advances of various functional materials and process techniques, nearly all kinds of passive and active electronic devices could now be realized by low cost and high throughput printing.

This presentation will firstly discuss the possibility of expanding "More than Moore" to address these challenges by combining advantages of the printed organic transistor and the silicon microelectronics. For the hybrid integration, the issues of large operation voltage with poor power efficiency with organic transistors manufactured by printing processes will be highlighted. Our research on various approaches, including enlarging the gate dielectric capacitance and reducing the channel sub-gap density of states, towards making fully printable organic transistors with low operation voltage will then be presented. Development of a compact device model with a simple extraction tool and circuit-level design techniques based on the organic transistors will also be discussed, which are important as part of the technology platform for constructing organic transistor circuits and systems.

Biography

Xiaojun Guo received the Ph.D. degree from University of Surrey (UK) in 2007, both in electronic engineering. He continued his stay at University of Surrey for one more year as a postdoc Research Fellow. Before joining Shanghai Jiao Tong University in Aug. 2009, he had been working in Plastic Logic Ltd., Cambridge, UK, on research and development of printed polymer TFTs backplanes for flexible displays, and technology transfer for manufacturing. His group is now focusing on device and integration of printable thin film transistors and functional devices including displays, sensors and memories. He has authored or co-authored more than 60 technical papers in international journals and conferences.

SESSION 2:

Manufacturing technologies 1

(2.1) Ultra-fast Fabrication of Printed Electronics Through Photonic Curing and Soldering

Rob Hendriks

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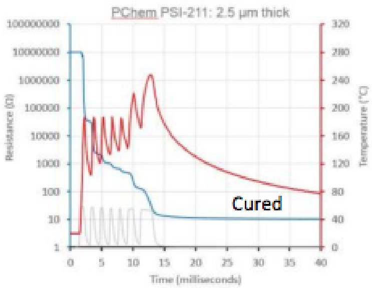
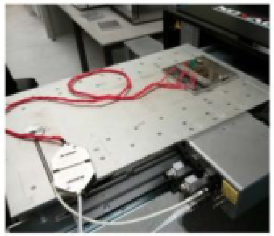
Abstract

As the demand for printed electronics is increasing, faster and cheaper processes are required to reduce production costs. In contrast to time consuming oven post-treatment steps, curing of conductive inks and soldering of components can be done within a fraction of a second by means of highly intense light pulses (photonic curing). This short processing time allows for high volume, cost effective and energy efficient production of printed electronics in a roll-to-roll manner. Photonic curing/soldering enables high temperature processing on temperature sensitive substrates such as PET and paper.

Keywords: photonic curing, photonic soldering, in-situ measurements, simulation, conductive inks





Measuring setup in a PulseForge 1300

Biography

After his studies, Rob Hendriks started working in the field of printed electronics at the Holst Centre in 2011. During this period he became the expert on photonic curing and the characterization of conductive inks. In 2013 he started the PhATT Project (Photonic Ablation & Transfer Technology), which focusses on the development of new technologies using high intensity light pulses, e.g. printing, soldering. Driven by the idea of commercialization of these new technologies, in 2014 he started working for NovaCentrix, the company which produces state-of-the-art photonic curing equipment.

(2.2) Roll to roll digital photolithography

Thomas Harvey[1], Richard Patterson[1], Peter Rippingale[1], Louise Evans[1], Simon Ogier[1], Gerrit Heuvelman[2], Simon Aigner[2], Roland Kaplan[2], John Rudin[3]

[1] Centre for Process Innovation Limited, Thomas Wright Way, NETPark, Sedgefield, TS21 3FG, UK [2]Heidelberg Instruments GmbH, Tullastrasse 2, D-69126 Heidelberg, Germany
[3]Folium Optics Limited, Unit 28, Cooper Road, Thornbury, Bristol, BS35 3UP, UK

The processing of rolls of 'free-standing' polymer film substrates has remained a major challenge for Organic Large Area Electronics. The existing approach is often to laminate polymer substrates to rigid carriers, and process through standard lithographic tools, which negates much of the benefit predicted for polymer processing. Mask based tools provide production rate throughput, but incur high NRE (non-recoverable engineering) costs associated with mask fabrication, and cannot adapt to dimensional changes beyond a few 100ppm, making overlay onto existing patterns very challenging. Purely digital systems are used for mask writing, typically on glass or film, but, typically have too low a data throughput (<1MPixel/s) to be suitable for use on a roll to roll tool.

We will report on the final results of a 3 year long joint European collaborative research project (acronym "Digilith"). The project had the objective of demonstrating the feasibility of a high resolution (~5um) UV photo imaging system which can operate at much higher throughput (~0.1m^2/min) on free-standing film. This requires an imaging engine that can provide rendering rates in the region of 1Gpixels/s, with power densities compatible with existing photoactive materials (such as photoresists and UV-curable resins), and film handling and transport mechanisms to ensure high accuracy overlay (<2um). During the project, we have built a prototype roll to roll digital photolithography tool and it is currently being tested at CPI. The tool is designed to expose rolls or sheets of film with a 20mm wide exposure field at a speed of up to 1.2 m/min. Digital images are generated using a Digital Micro-Mirror Array (DMD) working in combination with an 18W@50KHz Nd:YVO_4 laser source at 355nm. The design of the optical system has been done so as to minimise the cost of ownership of future equipment while maintaining the required resolution and aperture. The system tracks the film position using a combination of a high accuracy rotation encoder and an optical system which tracks QR codes printed onto the back of the carrier film web. Testing which will be carried out will include characterisation of organic thin film transistor (OTFT) devices made using the new tool.

Figure 1: The Digilith R2R digital exposure tool

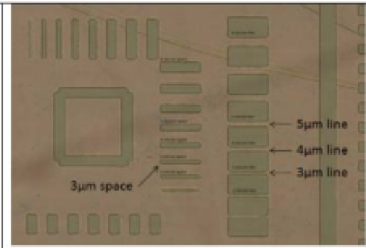


Figure 2: Resist image from Digilith tool

Keywords: photolithography, digital, imaging, organic, transistor

The **Centre for Process Innovation** (CPI) is part of the High Value Manufacturing Catapult and runs the UK National Centre of Excellence for Printable Electronics. CPI helps companies reduce risk and decrease time to market by demonstrating, refining or scaling-up novel technologies. CPI's facility in Sedgefield comprises 1500m^2 of clean room facilities with equipment able to process substrates up to 370mm x 470mm in size or rolls of film.

With an installation base of over 600 systems in more than 50 countries, **Heidelberg Instruments Mikrotechnik GmbH** is a world leader in production of high precision maskless lithography systems. Due to their flexibility, these systems are used in research, development and industrial applications for direct writing and photomask production by some of the most prestigious universities and industry leaders in the world.

(2.3) Photonic processes in printed electronics

Guy Bex[1], Rob Hendriks[2], Merijn Giesbers[1], Edsger Smits[1], Gari Arutinov[1], Jeroen van den Brand[1]

[1] **Holst Centre / TNO, High Tech Campus 31, 5656AE, Eindhoven, The Netherlands.**
[2] **NovaCentrix, 400 Parker Rd #1110, Austin, TX 78728, United States**

In recent years, the Printed Electronics industry has witnessed several impressive technological breakthroughs, effectively paving the way towards a wide range of novel processing methods and applications. At the same time, however, current production technologies are still heavily relying on traditional approaches for deposition and post-deposition treatment. This dependence on techniques like inkjet or screen printing and thermal oven curing results in a number of serious limitations for the resolution and accuracy of functional patterns as well as for a reliable device production on industrial scales. Innovative approaches for processing based on light, such as Laser Induced Forward Transfer (LIFT) and photonic flash sintering, have already demonstrated their high potential to supplement the Printed Electronics industry's toolbox. In this contribution, we will present our own efforts and results using these technologies for the printing and curing of functional electronic materials like electric conductors, insulators and conductive adhesives. In addition, a novel deposition method, the so-called Photonic Ablation and Transfer Technology (PhATT), will be introduced. Similar to LIFT, in PhATT setting light pulses applied from the backside through a transparent donor substrate are used to transfer functional materials onto an acceptor substrate using a non-contact approach. In contrast to LIFT, however, a high intensity Xenon flash lamp with a broadband emission covering the entire visible spectrum is used as a light source. More importantly even, patterning is achieved by a mask, which enables to simultaneous transfer of a large number of droplets with a single pulse. As a consequence, PhATT is proven to be extremely fast (areas of 5 by 5 square centimetres have been printed within 100 µs) and, especially in combination with rapid and selective post-deposition technologies like photonic flash sintering, has good prospects for being upscaled towards roll-to-roll production.

Biography

Guy Bex studied chemistry at Fontys University of Applied Sciences in Eindhoven. In 2014 he joined Holst Centre where he is currently working in the technology program "Printed Functional Structures on Flexible Substrates". His main research interests include photonic printing, curing and sintering technologies and process development for the Printed Electronics industry.

(2.4) Towards the in-line inspection of organic photovoltaic cells using surface-function correlation

Sebastian Wood,* Daniel O'Connor, Christopher W Jones, James Claverley, James Blakesley, Claudiu Giusca, and Fernando Castro

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***Corresponding author: sebastian.wood@npl.co.uk**

The economic viability of large-area electronics products such as organic photovoltaic (OPV) panels depends on the management of defects, both during the initial deposition process optimisation and the subsequent high-volume manufacture. Functional data is typically only obtained in the final stages of manufacture in the form of a globally measured cell/module efficiency. Here we show how to exploit correlation studies linking the final functional performance of a device to dimensional measurands (e.g. surface texture parameters), which can be acquired in-line, with a view to identifying which defects will be critical to the device functionality.

OPV device samples were fabricated with artificial defects, for example, silica microspheres to represent dust, in order to evaluate the inspection technique. The surface topography was surveyed layer by layer using a coherence scanning interferometer (see Figure 1(b-e)), which enabled us to characterise the defects and their impact on subsequently deposited layers.

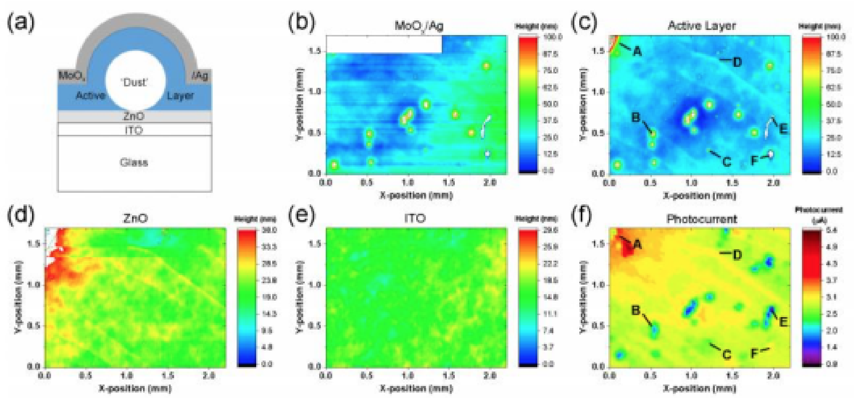


Figure 1. (a) Diagram indicating structure of OPV device showing a silica microsphere deposited to simulate dust (not to scale). (b-e) Surface topography of the same local region of the sample measured after each layer deposition using a coherence scanning interferometer (Height scales are zeroed to the minimum height measured for each layer, and missing values are represented in white). (f) Photocurrent map for the complete device. Various defects (A-F) are labelled in (c) and (f) to highlight the structure- function comparison.

The functional performance of the sample was characterised using a range of electro-optical techniques in order to observe local variations in the device performance (see map of photocurrent in Figure 1(f)). By identifying correlations between the surface texture parameters and the functional data it is now possible to predict the functional impact of defects and infer device performance using the more easily obtainable dimensional data alone. This knowledge can be used to specify tolerances for the surface texture parameters of the substrate materials and the subsequently deposited layers such that a certain device performance is achieved.

Keywords

Organic photovoltaics; Defect characterisation; Dimensional surface metrology; Surface- function correlation; Defect detection.

Biography

Sebastian Wood completed his PhD in 2014 with Dr. Ji-Seon Kim and Prof. Jenny Nelson at Imperial College London, studying the optoelectronic and morphological properties of conjugated polymers for use in plastic electronic devices, with a particular focus on the use of resonant Raman spectroscopy. He now works at the National Physical Laboratory developing novel spectroscopic and electrical measurement techniques to support the commercialisation of organic photovoltaics.

SESSION 3:

Energy harvesting and storage

Invited Speaker

(3.1) TITLE TBD

Prof Henry Snaith,

University of Oxford

Biography

Prof Henry J Snaith FRS leads a research group at Oxford University and is CSO and Founder of Oxford PV Ltd. His work is focussed on developing new materials for photovoltaics and understanding and controlling the physical processes occurring within the devices. He has made a number of advances and discoveries, with the most notable being the discovery of the remarkable PV properties of metal halide perovskites. He was awarded the institute of Physics Patterson Medal in 2012, named as one of "natures ten" people who mattered in 2013, received the Materials Research Society Outstanding Young Investigator award in 2014 and elected as a member of the Royal Society in 2015. In December 2010 he founded Oxford PV Ltd. which is commercialising the perovskite solar technology transferred from his University Laboratory, which in on track to deliver the highest efficiency lowest cost next generation PV technology.

(3.2) Printing of graphene nanoplatelets as low cost electro-catalysts for dye sensitised solar cells

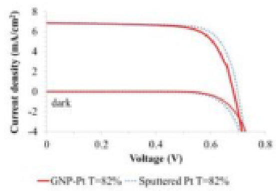
J. Baker[†], J.D. McGettrick[‡], D.T. Gethin[†], T.M. Watson[‡],

[†] Welsh Centre for Printing and Coating, Swansea University, UK
[‡] SPECIFIC, Swansea University, Baglan Bay Innovation Centre, Baglan, UK

Keywords: Graphene nanoplatelets, ink, roll to roll manufacture, dye sensitised solar cell, printing

Reverse illuminated flexible dye sensitised solar cells (DSCs) can be manufactured onto a titanium substrate using printing technologies which allow the production costs to be reduced. A key component of a DSC is the counter electrode catalyst which is typically platinum for iodide based electrolytes. To deposit robust platinum catalysts onto flexible transparent substrates, such as tin doped indium oxide - polyethylene terephthalate (ITO- PET), requires expensive vacuum based sputtering. Graphene nanoplatelets (GNPs) were used as the active material in a high surface area ink with viscosity of 20 mPas. The ink can be deposited onto an ITO-PET substrate by a number of inline printing methods, including flexographic printing[1]. By tailoring the GNP loading and binder content the ink can be optimised. The optimised ink had a transmission at 550 nm(T_{550}) = 85 % and an Rct of 6 Ω/□. Although the Rct is higher than required for laboratory cells with Jsc of 20 mA/cm^2 under 1sun test conditions it is sufficient for the lower (Jsc = 7 mA/cm^2 under 1 sun) Jsc of industrially produced reverse devices, especially when utilised for indoor applications where Jsc = 50 µA/cm^2 under 1000 lux. This is demonstrated by reverse illuminated DSC efficiencies with flexible cathodes which were equivalent to cells with sputtered platinum catalysts when under 0.5 sun illumination or less. To further improve the catalytic properties of the ink, platinum was thermally reduced onto the surface of the GNPs before manufacturing the ink[2]. Figure 1a shows that the performance of the GNP-Pt ink catalyst is comparable with sputtered platinum in a DSC. Figure 1b is a picture of a flexible DSC with printed catalyst which is a versatile low cost replacement for sputtered platinum on flexible substrates.

(a)



(b)

Figure 1a - JV curve comparing a GNP-Pt ink catalyst with platinum under standard test conditions, Figure 1b - Flexible DSC with printed catalyst.

References

1. Baker, J., Deganello, D., Gethin, D. T. & Watson, T. M. Flexographic printing of graphene nanoplatelet ink to replace platinum as counter electrode catalyst in flexible dye sensitised solar cell. *Mater. Res. Innov.* **18,** 86–90 (2014).
2. Baker, J., McGettrick, J. D., Gethin, D. T. & Watson, T. M. Impedance Characteristics of Transparent GNP-Pt Ink Catalysts for Flexible Dye Sensitized Solar Cells. *J. Electrochem. Soc.* **162,** H564–H569 (2015).

Acknowledgements

This work was part-funded by Haydale and the European Social Fund (ESF) through the European Union's Convergence programme administered by the Welsh Government. The authors would like to thank the EPSRC and TSB for supporting this work through the SPECIFIC Innovation and Knowledge Centre

Biography

From 2011-2014 Jenny Baker worked in the Welsh Centre for Printing and Coating developing graphene inks for dye sensitised solar cell applications. In 2015 she was awarded her PhD from Swansea University in nanotechnology with a thesis entitled 'Development and Characterisation of Graphene Ink Catalysts for use in Dye Sensitised Solar Cells'. Jenny currently works as the lead researcher investigating the printing and scale up of perovskite solar cells for SPECIFIC which is a consortium formed by Swansea University, Tata Steel, BASF and NSG Pilkington.

(3.3) Mass volume printing of energy harvesting device: development of antenna and tunable capacitor system.

Y. Mouhamad[*], N. Porter[†], L.G. Occhipinti[‡] and D. Deganello*

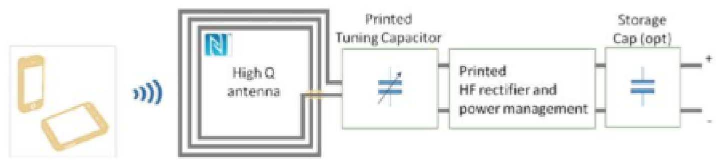
[*]Welsh Centre for Printing and Coating (WCPC), College of Engineering, Swansea University Bay Campus, Engineering East, Fabian Way, Swansea, SA1 8EN
[†]National Printable Electronics Centre, Thomas Wright Way, NETPark, Sedgefield, County Durham, TS21 3FG
[‡]University of Cambridge, Electrical Engineering Division, 9 JJ Thomson Avenue, Cambridge, CB3 0FA

The development of low cost printed energy harvesting device powered by near-field communication (NFC) would facilitate the wider adoption of NFC-enabled applications in consumer packaging, document and brand security. Other applications include wireless sensor networks for defence, healthcare and medical devices. The key technological challenge is the development of high gain antenna and tunable capacitor system to maximise the harvested power output. This work reports the ongoing development of an energy harvesting power module, in particular we will focus on recent advance on the printing and characterisation of specifically designed antennas and capacitors manufactured using high volume printing processes for an affordable mass-volume production.

Antennas were printed through a full-scale industrial roll to roll flexographic press. The morphology, the uniformity and the resistance of the antennas were studied for various antenna designs, plate patterning and orientations relatively to the printing direction. The antenna showed excellent height, track width and morphology consistency, with a significant improvement of on uniformity of antenna when the plate is patterned and rotated at 45° to the printing direction.

Newly designed capacitors were produced, these feature switchable interconnects for tunability. The capacitors were manufactured through screen printing, which achieved required deposit thicknesses and high resolution with features of 125um. The achieved capacitances conform to the predicted values and were in line with the requirements and showed excellent consistency.

The results showed huge potential for the proposed technology to be further explored. This work is part of the haRFest project funded by the Innovate UK, led by PragmatIC in partnership with CPI Innovation Services and EPSRC Centre for Innovative Manufacturing in Large-Area Electronics, represented by its academic partners University of Cambridge and the Welsh Centre for Printing and Coating (WCPC, Swansea University).



Biography

Dr Youmna Mouhamad has a bachelor's degree in physics and chemistry from the University of Aix-Marseille II. Having been awarded an Erasmus grant she spent the final years of her bachelor's degree in the University of Leeds. After this she continued in Leeds University obtaining a Master of Physics. She then joined the polymer physics group in Sheffield University obtaining a PhD in studying the dynamics and phase separation of spin coated films. With the aim of combining her interest in applied research and her knowledge in polymer physics she joined the Welsh Centre for Printing and Coating where she has been formulating piezoresitive, flexible or stretchable inks. She is currently working on the printing of an antenna and tunable capacitor system for an energy harvesting module as part of the haRFest project funded by Innovate UK.

(3.4) Powering the Internet of Things: Screen Printed Batteries

Pritesh Hiralal, Dilek Ozgit, Gehan A.J. Amaratunga

Electrical Engineering Division, University of Cambridge, 9, JJ Thomson Avenue, Cambridge, CB3 0FA
Pritesh.hiralal@cantab.net

There is a growing demand for thin, flexible and low cost energy storage devices that can accommodate into the form factor of large area printed electronics. Our group has recently demonstrated several nanomaterial based enhancements for zinc based batteries [1,2], which improve not only energy and power densities but also result in improved cyclability of zinc based batteries. Flexen, one of the Pathfinder projects, aims to formulate these electrodes onto screen printable versions. We hereby present some of our progress towards translating these developments onto a printable platform, as a preliminary step and demonstrator for scale up. Our approach is around the use of a zinc based aqueous chemistry which is inherently safe, and produces energy and power densities competitive with Li-ion.
The work spans around two well-known battery chemistries, a primary (non-rechargeable) zinc-manganese oxide chemistry and the rechargeable zinc-silver oxide chemistry. This latter battery, in which zinc and silver change from metallic to oxide states during charge and discharge cycles, uses silver oxide as the positive electrode (cathode), zinc as the negative electrode (anode) plus an alkaline electrolyte, usually sodium hydroxide (NaOH) or potassium hydroxide (KOH). We have been able to achieve about 250 cycles on a rechargeable battery as a result of the control of zinc dendrite formation. We now demonstrate results of the screen printed battery electrodes (with 3 electrode materials, Zn, Ag2O and MnO2) and their resulting performance as battery electrodes as a function of printing parameters such as film thickness and paste formulation. We demonstrate the viability of this chemistry as a printed, rechargeable battery. A preliminary printed device is demonstrated.
These printed electrodes open possibilities for the fabrication of flexible, rechargeable batteries with high energy densities, which would enable a number of novel concepts for consumer electronics.

[1] ACS Nano, 2010, 4 (5), pp 2730–2734
[2] ACS Appl. Mater. Interfaces, 2014, 6 (23), pp 20752

Biography

Dr. Pritesh Hiralal completed his Ph.D. from the Department of Engineering at Cambridge University on Nanomaterials for energy, from where he joined industry at the Nokia Research Centre working on high power energy storage, where he contributed to the scale-up of a printed supercapacitor. He has been inventor in 8 patents and co-authored over 30 journal publications and a book chapter. He is currently a Research Associate as at the University of Cambridge. In the last few years, he has acted as a consultant for several companies in the energy storage area.

SESSION 4:

Emerging materials for organic electronics

(4.1) Novel Low-Cost Conductive Layers for Printed Electronics

Harry Cronin[1,3], John Gregory[2], Martin Brown[2], Zlatka Stoeva[1], Maxim Shkunov[3], S Ravi P Silva[3]

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[2] Heraeus Noblelight Ltd., Cambridge, UK
[3] University of Surrey, Guildford, UK

Keywords: Photo-curing, printed electronics, rapid processing, low-cost inks, process development

Large-area electronics is an emerging industry, forecast to be worth $70bn by 2024 [1]. All large-area electronic devices require some form of electrical interconnection to the outside world. This is commonly achieved by the printing of metal nanoparticle-based inks, which reach the desired conductivity when sintered – usually by thermal means. However, such inks are costly due to the expensive fabrication of the nanoparticles, and often necessitate the use of volatile organic solvents which may be undesirable in an industrial context. Also, thermal sintering is a slow and energy intensive process. A promising alternative sintering technology is photo-curing, which employs high intensity visible light pulses. While this technology is known to be of use in sintering nanoparticle based systems, which benefit from significant melting point suppression compared with bulk material, larger flake inks are more challenging to sinter by this means owing to the higher required temperatures. We report the novel application of visible light photo-curing to water-based inks containing 1-3 µm sized flake silver, with a potentially significant cost advantage compared with nanoparticle equivalents.

We find that the conductivity of such inks approaches and in some cases matches that of typical nanoparticle inks after photo-curing. Furthermore, in a typical interconnect application employing screen printed silver lines, the yield of conductive patterns was increased from 46% untreated to 90% after photo-curing. Standardised adhesion testing showed no detrimental effect of photo-curing when used in an optimised regime.

SEM analysis reveals that the treatment is able to both cure the printed layer and increase the mean particle size, with evidence of neck formation between adjacent particles. This leads to improved percolation and higher conductivity. We speculate based on these observations that the physical mechanism for increased conductivity and yield may be localised skin effect melting, leading to necking of particles across voids in the printed structures, combined with curing and solvent removal. This hypothesis is further supported by our modelling work.

Photo-curing is a high throughput technique suited to roll-to-roll applications, which can be applied on a range of substrates without substrate damage. Example applications, including RFID antennae, are discussed, in which initial trials show a performance advantage arising from the photo-curing which could not be achieved by purely thermal means. This work results from a collaboration between DZP Technologies Ltd and Heraeus Noblelight Ltd, both of Cambridge.

[1] IDTechEx - Printed, Organic & Flexible Electronics Forecasts, Players & Opportunities 2014-2024

Biography

Harry Cronin is an EngD research engineer working jointly at DZP Technologies in Cambridge and the University of Surrey. Harry received his MSci in Physics from Imperial College London and started his doctoral research in 2013. His research is focused on materials and process development for printed electronics, with a focus on printed solar cells.

(4.2) Towards Highly Stable Polymer Electronics

Iyad Nasrallah[1], Mark Nikolka[1], Katharina Broch[1], Aditya Sadhanala[1], Michael Hurhangee[2], Iain McCulloch[2], Henning Sirringhaus[1]

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[2]Department of Chemistry and Centre for Plastic Electronics, Imperial College London, London SW7 2AZ, United Kingdom
E-mail: in234@cam.ac.uk

Abstract
Due to their ease of processing, organic semiconductors are promising candidates for applications in high performance flexible displays and fast organic electronic circuitry. Recently, a lot of advances have been made on organic semiconductors with surprisingly high performance and carrier mobilities exceeding those of amorphous silicon and approaching mobilities of polycrystalline silicon. Owing to a high degree of crystallinity and intrinsic grain-boundaries many organic semiconductors however lack the uniformity for large area applications in e.g. displays. Amorphous and semi-crystalline donor-acceptor polymers with high field-effect mobilities > 1cm^2/Vs [1] address this issue - however, recent evidence suggest a strong correlation between their crystallinity and stability, posing a major limit for their otherwise, promising application. Additionally, the operational stability as well as device uniformity of donor-acceptor co-polymers so far does not meet the requirements for large scale, high performance applications.

Here, we report a novel technique for dramatically improving the operational stress stability, performance and uniformity of high mobility polymer field-effect transistors by the addition of specific small molecule additives to the polymer semiconductor film. We demonstrate, for the first time, polymer FETs that exhibit stable threshold voltages with threshold voltage shifts of less than 1V when subjected to a constant current operational stress for 1 day under conditions that are representative for applications in OLED active matrix displays. The approach constitutes in our view a technological breakthrough; it also makes the device characteristics independent of the atmosphere in which it is operated, causes a significant reduction in contact resistance and significantly improves device uniformity. We will discuss in detail the microscopic mechanism by which the molecular additives lead to this significant improvement in device performance and stability.
[1] Venkateshvaran, Nikolka *et al.*, Nature, **515**, 384–388 (2014)

Biography

Dr. Iyad Nasrallah is currently a Research Associate working with Prof. Henning Sirringhaus at the Cavendish Laboratory, University of Cambridge, UK. He holds an MEng in Electronic Engineering with Nanotechnology from the University of York, UK. He completed his PhD under the supervision of Prof. Henning Sirringhaus at the University of Cambridge where he worked on characterizing and improving device stability of organic field-effect transistors. His work was conducted in collaboration with an industrial partner. Iyad's current research interests are in the methods of integrating organic circuitry into state-of-the-art electronic applications using novel materials and fabrication processes.

(4.3) Solution-processed high-*k* nanocomposite gate dielectrics for use in low-voltage field-effect transistors (OFETs): Studying the influence of surface functionalisation of nanoparticles

S. Faraji[1], M. L. Turner[1], L.A. Majewski[2]

[1] School of Chemistry, University of Manchester, United Kingdom
[2] Microwave and Communication Systems, University of Manchester, United Kingdom

Abstract
The search for solution-processed dielectric materials with a high dielectric constant value (so-called high-*k*) to enable realization of low-voltage organic field-effect transistors (OFETs) is becoming an increasingly attractive area of research for organic and plastic electronics. Typical solution-processed OFETs operate at voltages that are too high for use in wearable/portable electronic devices or notably as aqueous sensors ($V > 5$ V). To achieve OFETs with ultralow-operational voltages (< 1.5 V) suitable for low-cost, large-area electronics, high-capacitance, solution-processable gate insulators that form trap-free interfaces are essential.

High-*k* nanocomposite dielectric materials based on polymer matrices reinforced with high-*k* metal oxide nanoparticles combine the functionalities of polymers, such as low-weight, low-cost and solution-processability, with the unique features of the inorganic nanoparticles, e.g. small size and high dielectric constant. High capacitance of such nanocomposites enables operation of OFETs at (ultra-) low voltages[1]. However, nanoparticles have a strong tendency to undergo agglomeration followed by insufficient dispersability in the polymer matrix, degrading the properties of the nanocomposites. To improve the homogeneity and stability of nanoparticles dispersion in polymer matrices, it is essential to functionalize the surface of the nanoparticles with appropriate self-assembled monolayers (SAMs) to promote repulsion between nanoparticles, improve their dispersability and maximize dielectric properties of the ultimate nanocomposites.

In this work, nanoparticles of hafnium oxide (HfO_2) and barium titanate ($BaTiO_2$) are modified using various SAMs before incorporated into high-*k* polymer matrices such as poly (vinylidene fluoride-co-hexafluoropropylene) P(VDF-HFP) and cyanoethylated cellulose. Surface modification has resulted in increased dispersability and loading (wt %) of nanoparticles into polymer matrices without any obvious agglomeration. Nanocomposite dielectrics with high values of *k* are obtained. Moreover, compared to nanocomposites with non-modified nanoparticles, those with surface functionalized nanoparticles displayed reduced leakage current density and improved electrical properties in OFETs. Using solution-processed semiconductors, OFETs are fabricated with a nanocomposite bilayer gate dielectric in high yield (> 90 %) with negligible hysteresis and low operational voltage (< 1.5 V).

Keywords: High-*k* Nanocomposites, low-voltage OFETs, solution-processed gate dielectrics, surface modification.

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[1]S. Faraji, T. Hashimoto, M. L. Turner and L. A. Majewski, *Organic Electronics*, 2015, **17**, 178.

Biography

I am a research associate at the University of Manchester working on interdisciplinary projects. My areas of interest are namely solution-processed 2D crystals, low-voltage electronics with particular interest in hybrid dielectric materials and large-area printed electronics. My current project, under supervision of Dr Cinzia Casiraghi in the School of Chemistry, is a collaborative work on 2D crystals financed by 2DTech and University of Manchester Intellectual Properties (UMIP). Besides, I am following up the 'proof of principle' project I started in 2014-2015 to exemplify the claims in the patent on 'high-k dielectrics for low-voltage electronics'. The project was funded by UMIP and carried out at the Organic Materials Innovation Centre (OMIC). I have also worked along the team in Manchester on the iPESS (Integration of Printed Electronics with Silicon for Smart Sensor Systems) flagship project funded by the EPSRC Centre for Innovative Manufacturing in Large Area Electronics.

(4.4) Synthesis of Large Area Graphene for High Performance in Flexible Optoelectronic Devices

Emre O. Polat, Ravinder Dahiya*

Bendable Electronics and Sensing Technologies (BEST) Group, Electronics and Nanoscale Engineering, University of Glasgow, Glasgow, G12 8QQ, UK
***Corresponding author (E-mail: Ravinder.Dahiya@glasgow.ac.uk)**

This work demonstrates an attractive low-cost route to obtain high-quality graphene films over large areas by using the copper foils that are typically used as the negative electrodes in lithium-ion batteries.[1] We first compared the electronic transport properties of our new graphene film with the one synthesized by using commonly used copper foils in chemical vapor deposition (CVD). We observed a stark improvement in the electrical performance of the transistors realized on our graphene films. To study the optical properties on large area, we transferred CVD based graphene to transparent flexible substrates using hot lamination method and performed large area optical scanning. We demonstrate the promise of our high quality graphene films for large areas with ~400 cm^2 flexible optical modulators. We obtained a profound light modulation over a broad spectrum by using the fabricated large area transparent graphene supercapacitors and we compared the performance of our devices with the one based on graphene from standard copper. We propose that the copper used in the lithium-ion batteries could be used to obtain high-quality graphene at much lower-cost, with the improved performance of electrical transport and optical properties in the devices made from them.

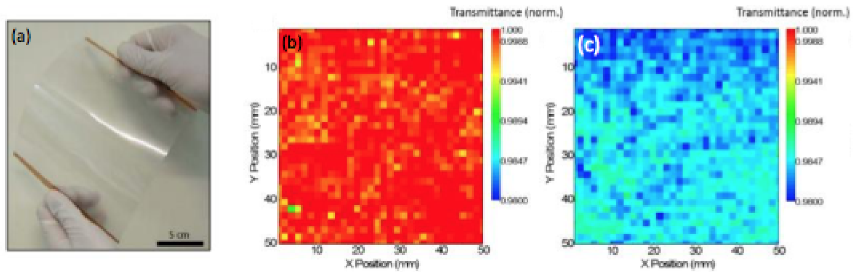

Figure 1. Optical characterization for the flexible graphene electrodes. (a) Photograph of the graphene transferred on PVC substrates by using hot lamination method. As an electrical contact pads, we protected the Cu lines at the edges of the sample during the etching. (b) Large area optical scan for a PVC substrate without graphene. We first scanned the reference substrate in x and y directions for 25 cm^2 area and mapped the normalized transmittance at 635 nm. (c) Large area optical scan for a graphene holding PVC substrate. After we transferred graphene on PVC, we performed the same large area optical scan and recorded the normalized transmittance and compared with the reference substrate.

Keywords: *Graphene, flexible, optoelectronics, smooth copper*

1. Emre O. Polat et al. "Synthesis of Large Area Graphene for High Performance in Flexible Optoelectronic Devices" Sci. Rep., doi: 10.1038/srep16744 (2015) (in publishment)

Biography

Emre O. Polat is a post-doctoral research fellow at University of Glasgow. His main focus is the integration of graphene on unconventional substrates which enables electronics and optoelectronic devices with new mechanical functionalities. He received his BSc. degree in physics from Izmir Institute of Technology, Turkey in 2009. And he got his Ph.D. degree in physics from Bilkent University, Turkey in 2015. His PhD research covers the graphene based optoelectronics. He showed for the first time a "Graphene Based Optical Modulator" working in visible wavelengths. Then by extending his research on multilayer graphene, he created "Graphene Based Flexible Smart Windows" that can change color with the application of voltage. He holds three patents and more than 10 publications in high impact factor journals. He is awarded for the "Young Scientist Award" of European Material Research Society (E-MRS) in 2014, and "Silver Leaf Award" of IEEE Prime in 2015.

Materials Synthesis and Process Engineering for Organic and Hybrid Opto-Electronics

Antonio Facchetti

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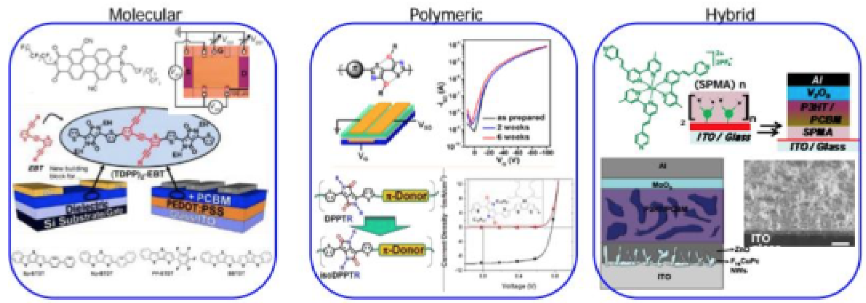
Email: a-facchetti@northwestern.edu

Printed opto-electronics is a new technology envisioning the fabrication of opto-electronic devices using printing methodologies. In this presentation I will describe the materials synthesis, development, and process engineering enabling the fabrication of unconventional opto-electronic devices, such as circuits and solar modules, all on flexible foils using several new materials.[1-3] Materials development include new synthetic, green routes to semiconducting polymers. Examples of unconventional electronic materials include organic small molecular and polymeric semiconductors, metal chelates and complexes, and hybrid organic-inorganic metal oxides. Thus, we will show the fabrication of polymer based complementary circuits with excellent performance (field-effect mobilities ~ 1-6 cm^2/Vs), amorphous oxides TFTs (field-effect mobilities ~ 5-40 cm^2/Vs) as well as polymeric donor-fullerene solar cells with efficiencies approaching 11% in inverted architectures.



(1) (a) Yu, X.; Zhou, N.; Lin, H.; Guo, P.; Smith, J.; Yu, J.; Chang, R. P. H.; Marks, T. J.; Liang, Y.; Chen, Z.; Jing, Y.; Rong, Y.; Facchetti, A.; Yao, Y. *J. Am. Chem. Soc.* **2015**, *137*, 4956-4959. (b) Facchetti, A. *Proc. Natl. Acad. Sci. U. S. A.* **2015**, *112*(11), 3217-3222. (c) Facchetti, A *Proc. Nat. Acad. Sci. USA* **2014**, (2014), *111(33)*, 11917-11918. (d) Facchetti A. *Materials Today* **2013**, *16*(4), 123-132.

(2) (a) X. Yu, L. Zeng, N. Zhou, P. Guo, F. Shi, D.B. Buchholz, J. Yu, V.P. Dravid, R.P. H. Chang, M. Bedzek, T.J. Marks, A. Facchetti *Adv. Mater.* **2015**, *27*(14), 2390-2399. (b) Fabiano, S.; Usta, H.; Forchheimer, R.; Crispin, X.; Facchetti, A.; Berggren, M. *Adv. Mater.* **2014**, *26*, 7438-7443.(c) Steyrleuthner, R.; Di Pietro, R.; Collins, B. A.; Polzer, F.; Himmelberger, S.; Schubert, M.; Chen, Z.; Zhang, S.; Salleo, A.; Ade, H.; Facchetti, A.; Neher, D. *J. Am. Chem. Soc.* **2014**, *136*, 4245-4256. (d) Usta, H.; Yilmaz, M. D.; Avestro, A.-J.; Boudinet, D.; Denti, M.; Zhao, W.; Stoddart, J. F.; Facchetti, A. *Adv Mater* **2013**, *25*, 4327-4334. (e) Lu, S.; Drees, M.; Yao, Y.; Boudinet, D.; Yan, H.; Pan, H.; Wang, J.; Li, Y.; Usta, H.; Facchetti, A. *Macromolecules* **2013**, *46*, 3895-3906. (f) Hong, W.; Sun, B.; Guo, C.; Y., J.; Li, Y.; Lu, S.; Huang, C.; Facchetti, A. *Chem. Commun.* **2013**, *49*, 484-48

(3) (a) Zhou, N.; Kim, M.-G.; Loser, S.; Smith, J.; Yoshida, H.; Guo, X.; Song, C.; Jin, H.; Chen, Z.; Yoon, S. M.; Freeman, A. J.; Chang, R. P. H.; Facchetti, A.; Marks, T. J. *Proc. Natl. Acad. Sci. U. S. A.* **2015**, *112*, 7897-7902. (b) Strappaveccia, G.; Ismalaj, E.; Petrucci, C.; Lanari, D.; Marrocchi, A.; Drees, M.; Facchetti, A.; Vaccaro, L. *Green Chem.* **2015**, *17*, 365-372. (c) Roland, S.; Neubert, S.; Albrecht, S.; Stannowski, B.; Seger, M.; Facchetti, A.; Schlatmann, R.; Rech, B.; Neher, D. *Adv. Mater.* **2015**, *27*, 1262-1267. (d) Guo, X.; Zhou, N.; Lou, S. J.; Smith, J.; Tice, D. B.; Hennek, J. W.; Ortiz, R. P.; López Navarrete, J. T.; Chen, L. X.; Chang, R. P. H.; Facchetti, A.; Marks T. J. *Nature Photonics* **2013**, *7*(10), 825-833. (e) Minder, N. A.; Lu, S.; Fratini, S.; Ciuchi, S.; Facchetti, A.; Morpurgo, A. F. *Adv. Mater.* **2013**, *25*, 4327-4334. (f) Fabiano, S,; Himmelberger, S,; Drees, M.; Chen, Z.; Altamimi, R. M.; Salleo, A.; Loi, M. A.; Facchetti, A. *Adv. En. Mater.* **2013**, 1301401-1301407.

Biography

Antonio Facchetti obtained his Laurea degree in Chemistry *cum laude* and a Ph.D in Chemical Sciences from the University of Milan. In 2002 he joined Northwestern University where he is currently an Adjunct Professor of Chemistry. He is a co-founder and currently the Chief Scientific Officer of Polyera Corporation. He is also a Distinguish Adjunct Professor of King Abdulaziz University and the Technology Advisor of Raynergy Tek Corporation. Dr. Facchetti has published more than 350 research articles, 11 book chapters, and holds more than 110 patents. He received the 2009 Italian Chemical Society Research Prize, the team IDTechEx Printed Electronics Europe 2010 Award, the corporate 2011 Flextech Award. In 2010 was elected a Kavli Fellow, in 2012 a Fellow of the American Association for the Advanced of Science (AAAS), and in 2013 Fellow of the Materials Research Society. IN 2010 he was selected among the "TOP 100 MATERIALS SCIENTISTS OF THE PAST DECADE (2000-2010)" by Thomson Reuters and in 2014 recognized as a Highly Cited Scientist. In 2015 he became a Fellow of the Royal Society of Chemistry and it has been selected as the 2016 ACS Award for Creative Invention. Dr. Facchetti's research interests include organic semiconductors and dielectrics for thin-film transistors, conducting polymers, molecular electronics, organic second- and third order nonlinear optical materials, and organic photovoltaics.

SESSION 5:

New market opportunities and technology trends (plenary)

(5.1) Thin film integrated circuits for IoT and sensor systems

Dr Tung-Huei Ke

imec, Kapeldreef 75, B3001 Leuven, Belgium

Abstract

As connectivity becomes ubiquitous in our lives, we start using electronics in a variety of everyday objects. We refer to the first examples as to the "Internet of Things" (IoT). The speed and extent of how IoT expands is defined by the functionality/cost scaling of its enabling IC components. In this presentation, Dr. Ke will share imec's vision of how thin-film electronics, as a new enabling technology for embedded IC, could facilitate the evolution of the "Internet of Things" into the "Internet of Everything". The vision will be supported by examples of concrete opportunities for thin-film IC components currently pursued by imec's industrial partners.

- Latest advances in thin-film IC component technologies (RFID/NFC, microprocessors, sensors, user-interfaces, etc.)
- Specific focus on RFID/NFC smart tags and sensors for consumer goods, packaging, and healthcare
- Phased approach to application development: custom design - prototyping - foundry manufacturing
- Leveraging FPD manufacturing facilities in a foundry mode

Company Profile (Imec)

Imec performs world-leading research in nanoelectronics. Imec leverages its scientific knowledge with the innovative power of its global partnerships in ICT, healthcare and energy. Imec delivers industry-relevant technology solutions. In a unique high-tech environment, its international top talent is committed to providing the building blocks for a better life in a sustainable society. Imec is headquartered in Leuven, Belgium, and has offices in Belgium, the Netherlands, Taiwan, US, China, India and Japan. Its staff of more than 2,200 people includes more than 700 industrial residents and guest researchers. In 2014, imec's revenue (P&L) totaled 363 million euro. Further information on imec can be found at http://www.imec.be

Biography

Tung-Huei Ke is a senior researcher in the Large Area Electronics department at imec, Belgium. He received Ph.D. degree at National Taiwan University in 2009. He was a visiting scholar at TU Dresden in Germany in Prof. Karl Leo's group with DAAD scholarship in 2007 and at Kyushu University in Japan in Prof. Chihaya Adachi's group in 2008. From 2011, Tung-Huei is with imec. He leads technology development projects in hybrid CMOS TFT ICs (organic and metal oxide) and in high-resolution photolithographic patterning for OLED displays. Tung-Huei authored over 20 conference contributions and journal publications on fundamental science and technology of thin-film electronics.

(5.2) Printed and Flexible Electronics in Wearables and Sensors

Dr Guillaume Chansin,

IDTechEx, Downing Park, Station Road, Swaffham Bulbeck Cambridge, CB25 0NW, UK

Abstract

This presentation will cover progress in printed and flexible electronics in wearable electronics and sensors. Some key market data and forecasts will be discussed. Based on new research from IDTechEx, the smart textile market will also be explored including case studies of new materials and devices coming to market.

Biography

Dr Guillaume Chansin is a Senior Technology Analyst at IDTechEx Research. Based in Cambridge (UK), he interprets the latest trends and market data in several industries, such as printed electronics, sensors, flexible displays and wearable electronics. Guillaume obtained a Diplôme d'Ingénieur in Physics Engineering at the Institut National des Sciences Appliquées (INSA) in Toulouse. His master's thesis was on three-dimensional fabrication with nanoimprint lithography. He went on to work on synthetic nanopore devices at Imperial College London, where he received his PhD. Guillaume has published several research papers in leading nanotechnology journals. His research has involved multiple disciplines such as nanotechnology, optics, microfabrication, microfluidics and materials science. Before joining IDTechEx, he worked on flexible e-paper displays at Plastic Logic. He is fluent in French and English and gives presentations in both languages. www.IDTechEx.com

Do sensors have a place in consumer packaged goods?

Dr Faiz Sherman

Procter & Gamble

Abstract

Not available

Biography

Dr. Sherman received a Ph.D. degree from the University of California, Los Angeles (UCLA) in 1998 with a specialty in MEMS technology. He also received his B.S. in Mechanical Engineering and M.S. in Nuclear Fusion from UCLA where he was a departmental scholar. In 2002, he graduated with an MBA from University of Cincinnati. Dr. Sherman joined Procter & Gamble (P&G) in 1998 to lead the MEMS R&D efforts in Corporate Research Division. He pioneered MEMS development area using plastic materials and mass production fabrication techniques. Dr. Sherman has led R&D efforts on cutting edge MEMS technologies for trans epidermal fluid sampling & drug delivery and sensor based technologies. During 2002-2008, Dr. Sherman initiated & has done extensive research on structural based Nanotechnology & activated chemistry. Recently, Dr. Sherman was appointed Fellow and has taken the technical leadership role in defining disruptive platform technologies for an up stream R&D organization. He is the author of 40+ patents.

SESSION 6:

Internet of Things and sensors

Invited Speaker

(6.1) Technologies towards digital paradise

Prof. Harri Kopola

VTT, Kaitoväylä 1, FI-90570 Oulu, Finland

Abstract

Not available

Biography

Professor Harri Kopola is Vice President Research in Knowlegde Intensive Products and Services Business Area at VTT Technical Research Centre of Finland Ltd. He is responsible of research strategy and research portfolio covering digital systems and services, communication systems, microsystems, intelligent sensors, metrology, printed functionalities and health. He received MSc and Doctor degrees in electrical engineering from University of Oulu. In 1989 he was postdoc at University of Ottawa. From 1990 to 1995 he was servicing University of Oulu as chief assistant and professor in electronics. He took 1995 research professor position at VTT, followed by positions as head of optoelectronics, research director and current position since January 1st 2014. As special initiative he led VTT spearhead program 'Center for Printed Intelligence' from August 2006 to December 2009. He had his expat period 4 months at the University of Tokyo 2012, and 8 months at the University of California Berkeley 2013.

(6.2) Activating surfaces: Flexible electronics for large-area sensors

Dr Tiziano Agostinelli

FlexEnable Limited, Cambridge | www.flexenable.com

The interest in shatter-proof, ultra-thin and flexible electronics has never been greater. According to IDTechEx, the printed, organic and flexible electronics market will be worth over $73 billion by 2025. This poses a challenge for technology providers to ensure adaptable and flexible prototyping and manufacturing capabilities that are able to quickly respond to the needs of end users.

Building on more than ten years' experience in flexible electronics, FlexEnable has developed one of the most disruptive technologies in recent years – a truly flexible transistor and electronics platform. We will provide an overview of our platform which combines stable high performance organic thin film transistors (OTFT) with passive elements to create truly flexible and cost effective electronics over large and small surfaces.This has led to the successful volume production of thin, lightweight and robust backplanes for flexible displays and sensors.

We will offer insight into our experience of developing flexible OLCD and OLED displays. Since we have demonstrated our groundbreaking OLCD platform we have had significant interest from product companies – particularly for wearables and automotive.

Example of FlexEnable's OLCD display curved around a coffee cup (left) and FlexEnable's transmissive backplane combined with ISORG's organic printed photodectors create the world's first X-ray imager on plastic.

Finally, we will explore applications of flexible electronics in sensors and imaging – another area we have experience in. Recent advances in the minimization of transistor off currents have enabled the detection of very small signals over large areas. This is particularly attractive for biometric applications, such as fingerprint sensors and digital X-ray flat panel imagers.

Biography

Dr Tiziano Agostinelli is a Senior Design Engineer at FlexEnable Ltd. He received Laurea degree and PhD in Electrical Engineering from the Politecnico di Milano, Italy. Following post-doctoral years at Imperial College of London and Plastic Logic Ltd, he joined FlexEnable Ltd in 2015. He has over 10 years' experience working in the field of plastic electronics and he is author or co-author of more than 20 papers on peer-reviewed international journals. He is inventor or co-inventor of 3 patents filed/awarded. His expertise covers the device physics, modelling and process optimization of organic photodetectors, solar cells and thin film transistors. His current interests are in the development of flexible backplanes and circuits for display and sensor applications.

(6.3) Fully solution-processed OFET platform for vapour sensing applications

E. Danesh [a], **S. Faraji** [b], **D. J. Tate** [c], **K. C. Persaud** [a], **L. A. Majewski** [b], **S. G. Yeates** [c], **M. L. Turner** [c]

[a] **School of Chemical Engineering & Analytical Science, The University of Manchester, Manchester, M13 9PL, UK**
[b] **School of Electrical & Electronic Engineering, The University of Manchester, Manchester, M13 9PL, UK**
[c] **School of Chemistry, The University of Manchester, Manchester, M13 9PL, UK**

Printed electronics is an emerging technology that enables development of low-cost, large-area electronic devices, such as flexible displays, RFID tags and environmental sensors, on a variety of substrates. Flexible plastic substrates are particularly attractive choices for such applications. However, they are incompatible with high-temperature processes used in conventional inorganic electronics. Polymeric dielectrics and semiconductors are promising candidates for printed electronics as they are mechanically flexible, and can be processed form solution. However, achieving high performance and high yields of devices using only solution processes remains challenging.

Here, we demonstrate a gas sensor array based on low-temperature, all solution-processed organic field-effect transistors (OFETs). Gate electrodes (width 200 μm) were patterned on a PEN substrate from a commercial silver nanoparticle-based ink using a Dimatix DMP-2831 inkjet printer, and sintered at 120 C. The gate electrodes were coated with an aqueous-based hybrid polymer-silica nanocomposite dielectric. This gate dielectric was cured at 120 C forming a robust cross-linked, chemically resistant and smooth layer (RMS roughness ~ 0.34 nm). Source and drain electrodes were inkjet printed to produce channel width and length of 2 mm and ~ 150 μm, respectively (Fig. 1a). Prior to the deposition of the semiconductor, surface treatments using self-assembled monolayers (SAMs) were carried out to adjust the work function of the silver electrodes, as well as the surface properties of the dielectric. Poly(3,6-di(2-thien-5-yl)-2,5-di(2-octyldodecyl)-pyrrolo[3,4-c]pyrrole-1,4-dione)thieno[3,2-b]thiophene) (DPPTTT) was used as the active layer of the sensing array. High field-effect mobility (1.0 $cm^2 V^{-1} s^{-1}$), high I_{on}/I_{off} ratio (> 10^3) and low hysteresis were achieved for the individual OFET devices of the array (Fig. 1b).

Ammonia was chosen as the analyte to exemplify the sensing capability of the platform, due to its relevance for environmental and health monitoring applications. NH_3 is a reducing gas and it decreases the number of charge carriers (holes) at the semiconductor-dielectric interface. The response of the sensor was therefore monitored as the change in the OFET's source-drain current (I_{ds}) upon exposure to various concentrations of ammonia. DPPTTT-based sensors showed sensitive and reversible room temperature (RT) response to ammonia vapour in air over the concentration range of 1-100 ppmv (Fig. 1c). The results demonstrated here further illustrate the potential of these OFET arrays in novel printed electronics applications, such as low-cost and low-power flexible sensors.

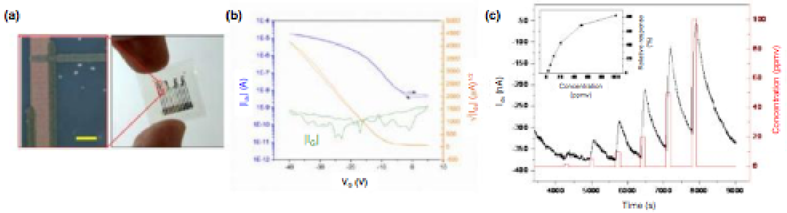


Figure 2. (a) Image of the sensing array consisting of 4 bottom-gate bottom-contact OFET elements. Inset shows part of the printed gate, source and drain electrodes (The scale bar is 200 μm) (b) Transfer characteristics of a device made using DPPTTT as the semiconductor (fabrication yield >90%). The green curve is the gate leakage current; (c) Transient RT sensor response towards a series of ammonia concentrations (1-100 ppmv) in dry air (V_g=V_{ds}=-20 V). The exposure and recovery times were 2 and 10 min, respectively. The inset shows the corresponding calibration curve.

References

[1] Fukuda, K. et al., *Nat. Comms.*, **2014**, 5, 4147 (DOI: 10.1038/ncomms5147)

[2] Tang, W. et al., *J. Mater. Chem. C*, **2014**, 2, 1995 (DOI: 10.1039/C3TC32134G)

[3] Faraji, S. et al, *Org. Electron.*, **2015**, 17, 178 (DOI:10.1016/j.orgel.2014.12.010)

[4] Li, J. et al. *Sci. Rep.*, **2012**, 2, 754 (DOI: 10.1038/srep00754)

[5] Danesh, E. et al., *Anal. Chem.*, **2014**, 86 (18), 8951 (DOI: 10.1021/ac501908c)

(6.4) Aerosol Jet® Printing of Antenna and Sensors for IoT

Michael J. Renn, Ph.D.

Optomec, Inc., 2575 University Drive, Suite 135, St. Paul, MN 55114 USA

Abstract

The demand for antennas and sensors printed directly onto products for the Internet of Things (IoT) is growing exponentially. While IoT applications are varied, common components for "Smart Connected Devices" include antenna and sensors. Printing technologies, such as Optomec's Aerosol Jet®, can enable rapid design turn-around, reduced manufacturing steps, and broader choices of target substrate and materials. Aerosol Jet is a high volume 3D printing solution for the production embedded electronic components. The process is non-contact, room temperature, and capable of patterning a wide variety of electronic and polymeric materials at the micrometer size scale. In the process, a liquid ink is aerosolized and the droplets are aerodynamically focused to a micron-scale point on the target substrate. The ink options include a wide range of off-the-shelf nanoparticle conductors, polymeric and inorganic semiconductors, ceramics, graphene, and other functional materials. Case studies involving production-scale printing of broadband, bluetooth, and NFC antenna along with strain and creep sensors will be presented. Material considerations, such as processing temperature, performance, and reliability will be discussed.

Key words: Aerosol Jet, 3D antenna, 3D sensors, 3D printing, IoT

Biography

Dr. Michael Renn is the Chief Technology Officer and Director of the Advanced Applications Laboratory at Optomec. He holds a B.A. degree from Lawrence University and a Ph.D. from the University of Virginia in physics. Dr. Renn was a postdoctoral fellow at the University of Colorado and an Assistant Professor at Michigan Technological University prior to joining Optomec in 1999. He and his team are responsible for materials, process, and applications development for Optomec's Aerosol Jet® technology.

SESSION 7:

Bio-electronics for smart wearable and implantable medical devices

(7.1) Organic Bioelectronics – new tools for medicine and biology

Prof. Magnus Berggren

Linköping University Dept of Science and Technology (ITN) SE-601 74 Norrköping, Sweden

First, printed electronics combined with organic bioelectronics and Si-chip technology aiming for future health care applications is reported. Printed e-labels including printed displays, antennas, dedicated sensors, energy harvesting and Si-chip technology for communication and signal processing have been realized. These e-labels have been further developed into skin-patches for the monitoring of critical health status parameters and as the communication node within a body communication network technology. With organic electronic ion pump circuits we can deliver biochemicals at high spatiotemporal resolution upon electronic addressing, thus enabling us to achieve local treatment and regulation of a vast array of physiological functions. With electronic skin patches, body area communication based on capacitive coupling and organic electronic drug delivery we suggest to establish a network in your body for the future health care to enable diagnostics, monitoring and treatment outside the hospitals.

Secondly, the roots, stems, leaves, and vascular circuitry of higher plants are responsible for conveying the chemical signals that regulate growth and functions. From a certain perspective, these features are analogous to the contacts, interconnections, devices, and wires of discrete and integrated electronic circuits. Although many attempts have been made to augment plant function with electroactive materials, plants' "circuitry" has never been directly merged with electronics. Here, we report analog and digital organic electronic circuits and devices manufactured in living plants. The four key components of a circuit have been achieved using the xylem, leaves, veins, and signals of the plant as the template and integral part of the circuit elements and functions. With integrated and distributed electronics in plants, one can envisage a range of applications including precision recording and regulation of physiology, energy harvesting from photosynthesis, and alternatives to genetic modification for plant optimization.

Biography

Magnus Berggren received his MSc in Physics in 1991 and graduated as PhD (Thesis: Organic Light Emitting Diodes) in Applied Physics in 1996, both degrees from Linköping University. He then joined Bell Laboratories in Murray Hill, NJ in the USA, for a one-year post doc period focusing on the development of organic lasers and novel optical resonator structures. In 1997 he teamed up with Opticom ASA, from Norway, and former colleagues of Linköping University to establish the company Thin Film Electronics AB. From 1997 to 1999 he served Thin Film as its founding managing director and initiated the development of printed electronic memories based on ferroelectric polymers. After this, he returned to Linköping University and also to a part time manager at Acreo Swedish ICT. In 1999, he initiated the research and development of paper electronics, in part supported by several paper- and packaging companies. Since 2002, he is the professor in Organic Electronics at Linköping University and the director of the Laboratory of Organic Electronics, today including close to 60 researchers. Magnus Berggren is one of the pioneers of the Organic Bioelectronics and Electronic Plants research areas and currently he is the acting director of the Strategic Research Area (SFO) of Advanced Functional Materials (AFM) at LiU. In 2012 Magnus Berggren was elected member of the Royal Swedish Academy of Sciences and in 2014 he received the Marcus Wallenberg Price.

(7.2) Soft bioelectronics for robotics and neuroprosthetics

Prof. Stephanie Lacour

École Polytechnique Fédérale de Lausanne (EPFL), Switzerland

Abstract

Repairing the human body is a formidable and overly ambitious task, which involves many disciplines and collaborative efforts. One of the challenges to overcome to deploy therapeutic neuroprostheses on and in the body lies in the physical mismatch between biological tissues and electronic circuits. The human body is soft, three-dimensional and in constant motion. Today's circuits are mostly planar and rigid chips, which need to be encapsulated to survive the harsh *in vivo* environment. This talk describes our efforts in narrowing this physical mismatch. We engineer sets of materials and mechanical designs to manufacture soft bioelectronics – large-area, thin-film electronic circuits with body-like, tissue-like behaviour. We illustrate the potential of this soft technology with examples ranging from prosthetic tactile skins to soft multimodal neural implants restoring locomotion following spinal cord injury.

Biography

Prof. Stéphanie P. Lacour holds the Bertarelli Foundation Chair in Neuroprosthetic Technology at the School of Engineering at the Ecole Polytechnique Fédérale de Lausanne. She received her PhD in Electrical Engineering from INSA de Lyon, France, and completed postdoctoral research at Princeton University (USA) and the University of Cambridge (UK). Her research focuses on the materials, technology and integration of soft bioelectronic interfaces including artificial skin and ultra-compliant neural electrodes for therapeutic neuroprosthetics. She is the recipient of the 2006 MIT TR35, a University Research Fellowship from the Royal Society (UK), a European Research Council ERC Starting Grant, a SNSF-ERC Consolidator Grant and was elected a 2015 Young Global Leader by the World Economic Forum. She is a member of EPFL Centre for Neuroprosthetics, http://cnp.epfl.ch.

(7.3) The opportunities of bioelectronics medicines as a treatment paradigm

Dr Roy Katso

GlaxoSmithKline, GSK House, 980 Great West Road, Brentford, London, TW8 9GS, United Kingdom

Abstract

The fact that we are living longer is resulting in increased disease burden and health costs that are posing some societal healthcare challenges with respect to the sustainability of the current model, to meet our needs in the medium to long-term. We are pursuing a new scientific field that could one day result in a novel class of medicines that would not be pills or injections, but miniaturised, implantable devices.GSK believes that the development of a new generation of implantable treatment modality termed "Bioelectronic Medicines potentially provides one of the solutions to address the aforementioned challenges. The envisaged closed-loop, miniaturised implantable devices, with the ability to discriminate between normal and pathological electrical signalling, will regulate pathological end organ functions of interest, with a tailored temporal and spatial precision that will complement or in some cases supersede current treatment modalities. This will result in a new paradigm of therapies for diseases such as diabetes, asthma and rheumatoid arthritis to mention a few that will address adherence, avoid broad system exposure, and consequently possess a superior efficacy. These miniaturised devices are envisaged to have a number of hallmarks; (i) they will target visceral peripheral nerves to modulate functions of organs central in major chronic diseases; (ii) they will selectively and intelligently modulate the neural code in discrete circuits; (iii) utilize pathological signatures to trigger tailored treatment intervention and; (iv) take a technology leap towards closed-loop, miniaturised devices. This presentation will outline the importance of building a global bioelectronics ecosystem and GSK's commitment to play its role in this emerging treatment paradigm.

Biography

My responsibilities in the Bioelectronics R&D Unit include identifying the best talent wherever it exits in the world and building new ecosystems in partnership with academics, technology companies, funding agencies and philanthropic organisations in order to accelerate the realisation of the delivery of the potential of Bioelectronic Medicines. This is done through an Open Innovation ethos and building partnerships that are multi-disciplinary in nature, co-exist in a complementary manner, and share a common vision of expediting delivering this treatment modality to address unmet patient need. An example of this is the Innovation Challenge where I am accountable for the identification and creation of global multi-disciplinary teams to undertake the development of an open access research platform with the ability to read, write and erase the neuronal language in visceral organs of interest. Such a common platform not only solves a major hurdle for the bioelectronic medicine research community, but also accelerates the technology development that may go into future manifestations of therapeutic devices that will be at the centre of new ventures and partnerships.

Previously, I received my Ph.D from Oxford University as a Rosina Valerie-Howell Fellow, where I studied the molecular mechanisms of an orphan receptor tyrosine-kinase in ovarian cancer. I spent two years at the University College London as a Ludwig Institute post-doctoral fellow, where my research focussed on the role of PI-3 kinases in cancer prior to joining GSK in 2001. I have worked for GSK for 12 years where I have lead multi-disciplinary matrix teams across a number of therapeutic areas and target classes in the early discovery of medicines. Prior to joining the Bioelectronics R&D Unit I worked in the R&D Strategy where I was accountable for providing decision support and program management for Pharmaceutical leadership on a number of key projects.

(7.4) Printed Epidermal Electronics

Matti Mäntysalo*, Thomas M. Kraft, Tiina Vuorinen

Tampere University of Technology, matti.mantysalo@tut.fi

Improving the cost-efficiency of public health-care is an important and significant challenge to overcome. To achieve this development, personal well-being, preventive health care, and a shift from expensive institutional care to home care is promoted. An underlying need for long-term monitoring of various physiological signals is common for all these areas. Although, it is common in today's state-of-the-art devices that only the sensor elements are integrated in clothing and that the main electronics are still in separate massive devices. Therefore, more user friendly solutions are needed, especially for remote-healthcare applications. Epidermal electronic systems (EES) represent a paradigm shift in wearable electronics which is enabled by recent advances in flexible and stretchable electronic technologies (e.g. printing). EES can conform to temporary transfer tattoos and deform with the skin without detachment or fracture.

In this seminar we will focus on printed ESS. We will present the fabrication and characterization of an intelligent, conformable, and user friendly physiological monitoring platform for continual nonintrusive wireless monitoring based on printed hybrid electronics.

Keywords: epidermal electronic system (ESS), printed electronics, stretchable electronics, wireless health node, internet-of-things

Biography

Matti Mäntysalo received his M.Sc. and D.Sc. (Tech) degrees in electrical engineering from Tampere University of Technology, Tampere, Finland in 2004 and 2008, respectively. He is an Asst. Prof. in Electronic Materials and has been awarded with the Adj. Prof. in digital fabrication at TUT. Mäntysalo has led the Printable Electronics Research Group at TUT since 2008. He was a visiting scientist in iPack Vinn Excellence Center, School of information and Communication Technology, KTH Royal Institute of Technology, Stockholm, Sweden, from 2011 to 2012. His research interests include printed electronic materials, fabrication processes, pre- and post-treatments, quality and performance analyses, reliability and failure analyses, and especially integration of printed electronics with silicon-based technology. Mäntysalo is active in IEEE CMPT, IEC TC119 Printed electronics standardization, and Hybrid System (spokesperson) working group in Organic Electronic Association.

SESSION 8:

Manufacturing technologies 2

Invited Speaker

(8.1) Advanced rheology for printing large area electronics

Prof. Rhodri Williams

Complex Fluid Research Group, College of Engineering, Swansea University, SA1 8EN

Abstract

The manufacture of complex structured products by flow-based processes, such as printing and coating, is of major industrial significance. Manufacturability, process control and, ultimately, product performance are critically dependent on the rheological behaviour of *complex fluids*. Advances in formulation to achieve successful manufacture in such processes demands appropriate levels of rheological information but such advances are presently constrained by a lack of appropriate rheological characterisation.

This paper reports work involving advances in rheometric characterisation which address two significant limitations of established rheometry based on small amplitude oscillatory shear (SAOS) in terms of its application to industrial, functional ink systems. The first limitation arises from the requirements of linear viscoelastic theory, which effectively restrict SAOS to the imposition of small (microscopic) deformations. The second limitation is the time required to complete material characterisation.

We report how these limitations are addressed using a novel exploitation of controlled stress parallel superposition (CSPS) rheometry, in which viscoelastic changes linked to the responses of material microstructures to large amplitude shear flow are probed. This CSPS rheometric technique is shown to be superior to existing rheometric techniques and to provide a new basis for establishing advanced rheological characterisation of complex materials under process relevant conditions. Reference is made to improved predictions of product outcome in print trials based on the new technique using a range of formulations of functional inks used in printed electronics manufacturing.

Biography

Professor Rhodri Williams works in the fields of non-Newtonian Fluid Mechanics, rheology, haemorheology, nanotechnology and cavitation with special reference to process/chemical engineering instrumentation and theoretical developments relevant to the liquid state. In 2012 he was awarded an Enterprise Fellowship by the Royal Academy of Engineering for his development of new blood clot diagnostics and sensors. He is President of the British Society of Rheology (2013-2015) and lead author of over 130 papers. His work has also led to recognition though major awards from the Royal Society (Brian Mercer Award), the Institution of Chemical Engineers (IChemE) Industry Award for Innovation and Excellence, the Annual Award of the British Society of Rheology and the ICI/AkzoNobel Strategic Technology Award.

(8.2) Manipulation and control of spatial ALD layers for flexible devices

Dr Dana Borsa

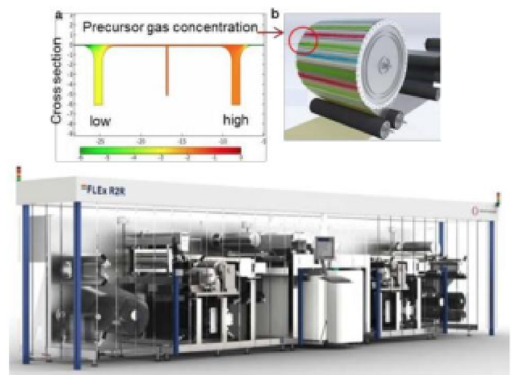
Meyer Burger (Netherlands) B.V., Luchthavenweg 10, 5657 EB Eindhoven, The Netherlands

During the past years there has been an increasing interest for flexible materials with advanced functionality. A new generation of flexible electronics can benefit from accurate control of coating thickness and material properties and also from combined inorganic/organic coating methods that can be integrated in one system. To serve this purpose, we have developed in collaboration with leading institutes in the Netherlands an innovative system that combines a highly controlled spatial ALD deposition system with a coatings step of an organic-based layer of method of choice, either patterned or fully covered.

Special attention has been given to designing a scalable segment-based injector head that can be applied for a roll-to-roll configuration but also for a rotary reactor. Moreover, this design allows for scalability in width but also in process speed and in the choice of precursor materials if a multilayer-like deposition configuration is envisioned. From gas flow modelling on a COMSOL platform insight into the foil transport and gas separation has been gained which could be directly transferred into the design of the equipment.

We will present how roll-to-roll spatial ALD enables production of high performance barrier foil which can be used to protect sensitive flexible electronics like OLEDs, thin film (O)PV and quantum dot foils. We will explain the basics of spatial ALD, the challenges of scaling up to industrial production and present an evaluation of the barrier and optical properties of deposited barriers. While a barrier of only 20 nm aluminium oxide (AlOx) does not change the foil optically, calcium degradation tests as well as MOCON-like measurements reveal a water vapor transmission rate as lowas $6\cdot10^{-5}$ g/m^2/day at 20°C and 50% relative humidity. Such an AlOx barrier is roll-to-roll deposited on regular 125 micron PET foil without any additional treatment.

The versatility of the roll-to-roll spatial ALD system is ideal for process and equipment development and represents an important milestone for fabrication of flexible solutions for various industries. Additional to barrier foils, such a system can also be used to deposit buffer layers and conductive oxides for CIGS, oxide semiconductors for TFT's or electrode materials for batteries. Moreover, with all processes at atmospheric pressure, we have opened the way to low cost production of flexible materials with advanced functionality.



Keywords
ALD, flexible electronics materials, simulations, R2R, production systems

Biography
Dr. Dana Borsa is Manager Research of the Thin Film Coating and Projects Business Unit at Meyer Burger (Netherlands) B.V. She is responsible for all process and application developments. Her PhD in physics from the Rijks Universiteit Groningen was focused on the growth and characterization of nitride- based thin films and multilayers. After some years of research on switchable mirrors and hydrogen storage materials at the Vrije Universiteit Amsterdam she moved to ECN and worked on high efficiency solar cell concepts before joining OTB Solar (currently Meyer Burger (Netherlands) B.V.) in 2009.

(8.3) Assessing the Scalability of Adhesion Lithography towards Highly Efficient Co-planar Nanogap Rectifying Diodes

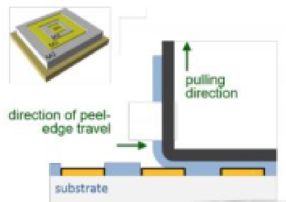
Dimitra G. Georgiadou, James Semple, Gwenhivir Wyatt-Moon and Thomas D. Anthopoulos

Physics Department, Imperial College London, London, United Kingdom

Keywords: plastic nanoelectronics, wireless communications, RF diodes, large area manufacturing, self-assembled monolayers

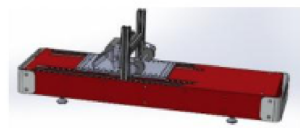
Adhesion lithography (a-Lith) is a novel patterning technique, which enables the manufacturing of large aspect ratio (>100,000) metal electrode nanogaps (<30 nm) on different material and area substrates in a controlled manner with high yield and at low cost. A-Lith relies upon the effective tuning of the adhesion forces developed between two similar or dissimilar metals by attaching a self-assembled monolayer (SAM) on the pre-patterned surface of the first metal layer (M1). Then, deposition of a second metal (M2) and its subsequent selective removal, with the aid of an adhesive material (sticky tape or glue), results in an M1/M2 lateral structure, where the two metals are separated by a 15-30 nm gap. Deposition of a suitable semiconducting material with high mobility and appropriate energy levels in the nanogap can then give rise to Schottky diodes with large rectification ratio and fast dynamic response at high operating frequencies, rendering these nanostructures ideal platforms for highly efficient rectifiers and other ambipolar devices.

The key process step in obtaining reliable nanogap structures with high throughput in industrially relevant dimensions (large areas) and on technologically attractive (flexible) substrates is the peeling of the adhesive material off the SAM-modified parts of the M2 surface. Process parameters such as peeling speed, angle, direction or force can substantially affect the quality of the co-planar metal electrode nanogaps.



D. J. Beesley, J. Semple, L. K. Jagadamma, A. Amassian, M. A. McLachlan, T. D. Anthopoulos and J. C. deMello, *Nature Communications* 5, 3933 (2014)

To this end, we have designed and developed a semi-automated peeling system to control and optimise the above process parameters, and also effectively assess the scalability potential of the a-Lith nanogap electrodes fabrication, enabling thus the fast and robust manufacturing of devices of interest.



Herein we demonstrate - as a *proof-of-concept* application - radio frequency rectifying Schottky diodes that can drive high currents in a very small active area due to the extreme downscaling of key device dimensions obtained *via* this innovative patterning technique. In particular, it is shown that high aspect ratio nanodiodes with total widths ranging from 1cm to 1m can be fabricated with a-Lith on large areas and lead to high power outputs with cut-off frequencies exceeding the 13.56 MHz benchmark for near field communications (NFC) and other power applications. This ideal combination of *scalability vs capability* renders this exemplary manufacturing method unique within the field of plastic electronics.

Biography

Dr Dimitra G. Georgiadou is a Postdoctoral Research Associate in the Experimental Solid State Physics group (EXSS) at the Blackett Laboratory, Imperial College London. She is currently working under the supervision of Professor Thomas Anthopoulos on the EPSRC-CIMLAE's "PLANALITH" project. Dimitra received her PhD in Photochemistry/Organic Electronics from the National Technical University of Athens. Before that she obtained a Master's Degree in Advanced Materials Science from the Technical University of Munich, Ludvig-Maximilians University of Munich and University of Augsburg. She has also gained industrial experience through internships in Procter&Gamble, Italy, and Schreiner Group, Germany. Dimitra is co-author of over 35 publications in peer-reviewed journals (h-index: 14).

(8.4) Production and measurement of roll-to-roll ALD barriers for electronic applications; results from FP7 projects R2R-CIGS and NanoMend

David Bird

The Centre for Process Innovation (CPI) Limited, Thomas Wright Way, NETPark, Sedgefield, TS21 3FG

Key words: ALD, barrier, roll-to-roll, NanoMend, R2R-CIGS.

The use of organic electronic materials, combined with the desire to produce lightweight & low cost flexible devices, raises the need to develop a commercially viable technology which limits the impact of the active material's intrinsic environmental instability.

CPI has been involved in the area of barrier film and encapsulation development for many years and with its recent acquisition of R2R Atomic Layer Deposition (ALD) capability is actively engaging with the industry to meet this technology need. This presentation reviews the existing technologies highlights the barrier and associated metrology technologies being developed at CPI's National Printable Electronics Facility, including a variant of calcium-test which has been calibrated to the mass standard.

The challenges of testing an ultra-barrier material over large areas are significant, as are identifying defects of significant size; holes or coating defects in an optically transparent, <100 nm thick layer are difficult to find and measure without making a functional device, taking days, then testing it with accelerated ageing, which can take weeks. Data from the EU-FP7 projects NanoMend and R2R-CIGS documents the developments from a temporal-ALD batch process to a roll-to-roll spatial-ALD process.

Included is the development of a roll-to-roll inspection method based on wavelength scanning interferometry that allows the morphology of the surface of 0.5 m wide polymer films to be examined without affecting the quality of the roll and so allowing subsequent processing.

The aim of this work is to reduce costs and improve the manufacturability of these materials for a commercial/industrial environment.

Biography

Dr David Bird has 11 years experience working with film substrates and barrier materials. David completed an Engineering Doctorate in 2008 sponsored by DuPont Teijin Films on nano-scale coatings on films for flexible electronics. Joining CPI in 2008, he is now a Principal Scientist at the UK's National Printable Electronics Centre, focussing on vacuum-deposition of barrier materials. In 7 years at CPI David has 23 IP submissions (for Patent, Publication or internal Know-how), 17 of which relate to Barrier Materials and their integration to functional devices.

Biography

Dr Dimitra G. Georgiadou is a Postdoctoral Research Associate in the Experimental Solid State Physics group (EXSS) at the Blackett Laboratory, Imperial College London. She is currently working under the supervision of Professor Thomas Anthopoulos on the EPSRC-CIMLAE's "PLANALITH" project. Dimitra received her PhD in Photochemistry/Organic Electronics from the National Technical University of Athens. Before that she obtained a Master's Degree in Advanced Materials Science from the Technical University of Munich, Ludvig-Maximilians University of Munich and University of Augsburg. She has also gained industrial experience through internships in Procter&Gamble, Italy, and Schreiner Group, Germany. Dimitra is co-author of over 35 publications in peer-reviewed journals (h-index: 14).

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The aim of this work is to reduce costs and improve the manufacturability of these materials for a commercial/industrial environment.

Biography

Dr David Bird has 11 years experience working with film substrates and barrier materials. David completed an Engineering Doctorate in 2008 sponsored by DuPont Teijin Films on nano-scale coatings on films for flexible electronics. Joining CPI in 2008, he is now a Principal Scientist at the UK's National Printable Electronics Centre, focussing on vacuum-deposition of barrier materials. In 7 years at CPI David has 23 IP submissions (for Patent, Publication or internal Know-how), 17 of which relate to Barrier Materials and their integration to functional devices.

(8.5) Implementation of a linear optical encoder for high precision in line position referencing of plastic film in a Roll-to-Roll system

Kai Hollstein,[1] Daniel O'Connor,[2,*] Christopher W. Jones,[2] Paul Morantz[1] and Paul Comley[1]

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Keywords
Flexible substrate alignment; Optical encoder; Dimensional metrology; Testing and system integration challenges.

Abstract

The EPSRC Centre for Innovative Manufacturing in Ultra Precision is developing a large scale Reel-to-Reel (R2R) film fabrication research platform. This R2R research platform is aimed at processing 1.2 m wide films at accuracy levels and processing speeds previously not achieved. Novel means of measuring and controlling the flexible substrate's position and shape state are required to enable closed-loop web steering systems for the control of fabrication processes. For some processes it may be sufficient to infer the position of the web by tracking the motion of the rollers using rotary encoders since the web nominally follows this motion; however, the translation, slippage and stretch of the web material in two dimensions over the rollers prevents truly high precision control. Direct monitoring of the web is therefore required.

We present the concept and experimental realisation of a linear optical encoder head adapted to track the in-plane motion of surface relief gratings embossed directly into a polyethylene terephthalate (PET) substrate. This is achieved by extracting signals in quadrature from a fringe pattern created by projecting coherent light through the grating. Figures 1(a, b) show an example fringe pattern and the associated Lissajous figure captured from the encoder. Figures 1(c-e) show the sub-micrometre measurement performance achieved by the developed encoder as determined by comparison with a reference encoder that is embedded in the stage used to simulate the linear motion.

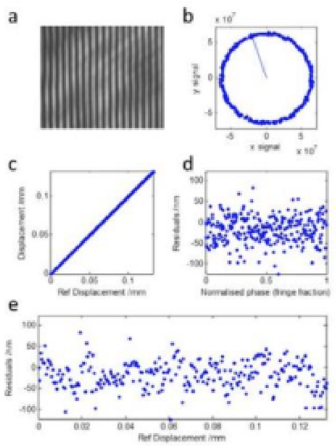

Figure 3 Tracking of a 16 μm period phase grating moving over a distance of 130 μm. Here, the encoder is triggered by a signal from a reference encoder every 500 nm. a) Example fringe pattern. b) Extracted Lissajous figure. c) Measured versus reference displacement. d) Fringe periodic displacement residuals. e) Displacement residuals.

Biography

D. O'Connor was admitted to the degree of Doctor of Philosophy in Physics at the Queen's University of Belfast in 2010. He has held postdoctoral positions at the Queen's University of Belfast and subsequently, at King's College, London. In 2013, he became a visiting assistant Professor in the physics department of the University of North Florida. Since 2014 he has held the position of Higher Research Scientist in the Engineering Measurement division of the National Physical Laboratory in Teddington, UK. His current research interests are in the design and implementation of optical systems for dimensional surface metrology.

WORKSHOP

Lasers for additive and subtractive LAE manufacturing

(W.1) Laser Direct Writing of large area electronics on flexible substrates

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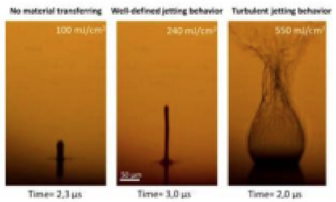
The increasing interest for organic and large area electronics has enabled the advent of novel microfabrication techniques. Among a large number of additive microfabrication processes, Laser Direct Write (LDW) techniques, such as Laser Induced Forward Transfer (LIFT), Selective Laser Patterning and Sintering of metal nanoparticle (NP) ink layers, stand out owing to their potential for printing uniform and well-defined conductive patterns with resolution down to 1μm on almost any type of substrate. In this work, we study the printing type regimes and resulting printing quality during the laser printing of copper (Cu) nanoink, which is a representative metallic nanoink for interconnect formation. Three regimes are identified: no material transferring, well-defined jetting, and undesirable jetting with a bulgy shape or plumping/splashing (Figure 4a). We then report on the printing and laser sintering of silver (Ag) nanoinks resulting in an electrical resistivity of 10 μOhm.cm. Finally, we demonstrated the use of LIFT technique for the fabrication of all laser printed resistive gas sensors consisting of reduced graphene oxide as sensing element, Ag nanoink both as electrode and electrical interconnect (Figure 4b) for the wire bonding of the operating device with the printed circuit board (PCB) on flexible (polyimide, PI) substrates. Next, graphene oxide in aqueous solution (4 mg/ml) was laser printed and thermally reduced on the pre-deposited electrodes, to provide the sensing element of the device. The printed devices were characterized by Optical Microscopy, SEM, electrical measurements and Raman Spectroscopy. Finally, the sensors were electrically characterized. The sensors exhibited good response upon the flow of humidity vapors (for humidity concentrations as low as 500ppm), with distinct resistance variations.

a)



b)

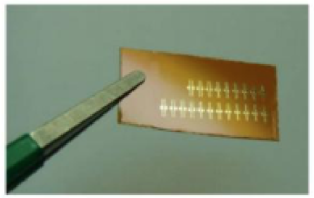


Figure 4: a) Printing type regime of Cu nanoink, b) laser printed Ag electrode pairs

Keywords: laser printed electronics, laser sintering, metal nanoparticles

Biography

Ioanna Zergioti is an Associate Professor at the National Technical University of Athens, School of Applied Mathematics and Physical Sciences. She studied Physics at the University of Crete and she received PhD at the Foundation for Research and Technology-Hellas. In the framework of her PhD work she worked for the fall semester of 1996 in the Mechanical Engineering Department at the University of California, Berkeley on the Laser Materials Processing. After her PhD, she worked as a post doctoral researcher in the Max Planck Institut für Biophysikalische Chemie in Göttingen. Then, she worked as a post-doctoral researcher in the Philips CFT until 2000. She was a researcher for 4 years (1999-2003) at the Laser Applications Division of the Institute of Electronic Structure and Laser – FORTH. Since September 2003 she was appointed at the National Technical University of Athens, School of Applied Mathematical and Physical Sciences. Her main activities are related to the laser processing and spectroscopy for electronics and biomedical applications. She has co-authored more than 80 publications in international refereed journals, 90 publications in conference proceedings, 4 chapter in scientific books, 3 granted Greek patents, 1 European patent. She has co-organised large conferences such as CLEO, EMRS, COLA conferences. She is currently coordinating two European Research projects, a Marie Curie IAPP "LaserMicroFab" and an ICT "BIOFOS".

(W.2) Recent advances in laser processes to print electrical connections: towards industrialization

E. Biver[1 *], C. Pasquier[1], S. Papazoglou[1], F. Zacharatos[2], St. Leyder[3], M. Makrygianni[2], R. Geremia[1], D. Puerto[3], A.P. Alloncle[3], Ph Delaporte[3], D. Karnakis[1] and I. Zergioti[2]

[1] **Oxford Lasers Ltd, Unit 8 Moorbrook Park, Oxfordshire, OX11 7HP, United Kingdom**
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[3] **Aix-Marseille University, CNRS, LP3 – UMR 7341, 13288 Marseille cedex 9, France**

Laser-based processes have been receiving a lot attention in recent years for 3D-printing applications. But do they have a place in the Large Area Electronics environment? Many groups are striving to bring laser printing of electrical connections from lab to market, making it compatible with industrial production standards.

Laser Induced Forward Transfer (LIFT) is a Direct Write processing technique which can print uniform and well-defined conductive patterns from almost any material in liquid or solid phase on various substrates. To print electrical connections, two approaches can be considered: (A) LIFT of a solid metallic layer, in which one or more absorbed laser pulses locally melt a thin donor layer and deposit droplets to an adjacent positioned receiving substrate. Connected such droplets form a conductive line; (B) LIFT printing of metallic nanoparticle inks in liquid form. Each method has advantages and drawbacks. LIFT of inks is more flexible but requires a post-processing sintering step to evaporate the ink solvent, melt (fuse) the nanoparticles and turn the printed patterns into a highly conductive circuit. This can be done by conventional oven or photonic curing. Another attractive method is laser sintering which is fast (typical scan speed meter/sec) and highly selective. It fully protects the substrate from heat-induced damage commonly encountered with other sintering techniques.

In this paper we focus mainly on LIFT printing of wet inks and laser sintering. Based on our recent work, we discuss several ways to implement these techniques in industry, review the challenges one needs to overcome and possible solution routes. We need to consider aspects such as the choice of ink (especially the type of metal and the viscosity), the donor preparation method, the laser properties, the incident laser beam spatial intensity shape as well as automation/handling issues.

Focusing on a sheet to sheet printing, we show that the thickness of the donor LIFT print layer from which the printing is made is a critical parameter. Therefore, to obtain an industrial standards process reproducibility matching industrial standards, the ink viscosity and donor deposition method on the donor substrate need to be carefully controlled. The incident beam intensity profile shape of the laser beam also has a big impact on the printing and sintering quality. We show that tailored beam shaping improves dramatically the process reproducibility and expands the working windows in term of writing speed and energy requirements. We evaluate the morphology (see Figure 1) and conductivity of the printed features. Finally, we discuss the key methods and components needed to build a robust laser-printing system based on these techniques.

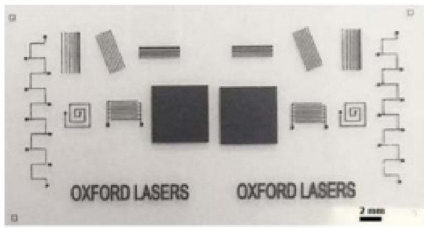

Figure 1 –Test Vehicle, laser-printed from a Silver nanoparticles ink, showing the potential of laser processes to print electrical connections.

Biography

Emeric Biver has an international engineering Master's Degree in Micro and Nanotechnologies for Integrated Systems and a Ph.D. on "Laser processes for the development of 3D-System In Package microelectronics". He worked on both laser ablation of polymers and Laser-Induced Forward Transfer (LIFT) of metallic nanoparticles inks. He is now working in the Research and Development team of Oxford Lasers, a laser micromachining company. His work involves laser printing and sintering, and laser platform development.

(W.3) Laser and inkjet tools for large area electronics manufacturing

Adam Brunton

M-Solv Ltd, Oxonian Park, Kidlington, Oxon, UK

In conventional silicon-based electronics, the manufacturing tools and processes are well-defined, more or less standardised and only advance in an incremental and conservative way. These tools are extremely sophisticated and very expensive. At the moment, however, there is no such definitive toolset for large area electronics manufacturing and, of course, the great opportunity for LAE is to combine low cost toolsets and processes to open up new applications and products.

Inkjet materials deposition and laser processing by, for example: ablation, modification, sintering or material transfer are rather complementary techniques as they are implemented on very similar machine platforms and are compatible with high-speed sheet to sheet or roll-to-roll processing, if necessary in controlled environments (clean, low H_2O, low O_2). Moreover they are both fully digital techniques – driven entirely from CAD files with no "hard tooling" required.

Here, we present some applications of combining laser and inkjet processes for manufacturing large area electronic devices such as capacitive touch sensors and thin film photovoltaic interconnects using a single pass instead of the more conventional multi-step process. Touch sensors are of particular interest as they are in industrial production for bespoke applications in our UK factory where the high product mix means a digital approach is highly advantageous. We can reliably define conducting, insulating and bridged structures ("2.5D") with dimensions of order 10 range of materials on a range of substrates which are generally applicable to LAE.

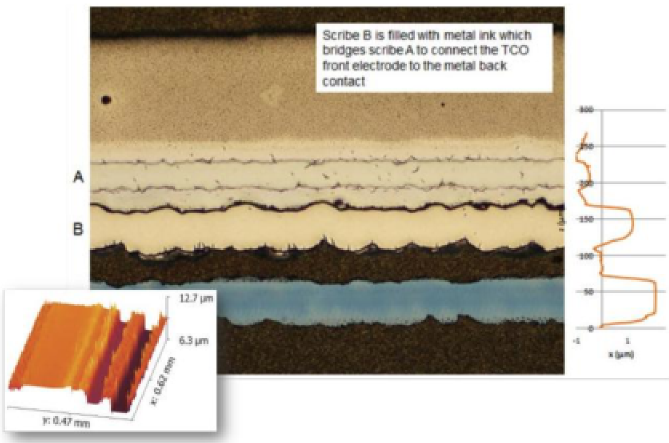

Figure 5: Thin film PV interconnect using: depth-selective laser scribes to expose required layers in the device; an inkjet-deposited insulating barrier to separate the cells and an inkjet-deposited conducting bridge to connect the cells from positive to negative.

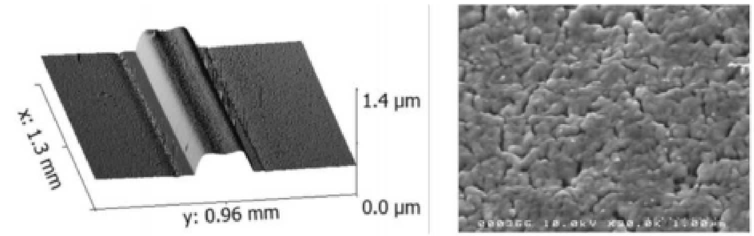

Figure 6: Conducting nano-silver inkjet printed track after localised sintering by high-speed scanning laser. Right: rendering from white-light interferometer data; left: SEM image showing high level of integrity in sintered material.

(W. 4) Laser Annealing of indium gallium zinc oxide: A platform towards flexible and large area processing of thin film transistors

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With a growing interest in flexible and transparent devices it is important to develop methods of fabrication that can meet the criteria relevant to large area electronics field. Laser Annealing (LA) is an excellent candidate for processing of thin films: LA is an ultra-fast and macroscopically cold process, which can be used in conjunction with temperature sensitive substrates. In addition, a laser beam can be moved and manipulated to process large areas and can have high spatial resolution for selective patterning / annealing. Thus, LA is a process of high value for flexible electronics in large-scale approaches (e.g. R2R). In this work, we investigate the application of Laser Annealing on Indium Gallium Zinc Oxide (IGZO) for thin film transistors.

a-IGZO thin films (200 nm thick) were deposited by radio frequency magnetron sputtering at room temperature. Then the IGZO thin films were subjected to a single nanosecond pulse LA at room temperature in atmosphere, using a KrF excimer laser (emitting light at 248 nm). A moderate range of fluences (50 to 125 mJ/cm2) was applied to the samples. IGZO thin films demonstrated a significant resistivity reduction upon processing, while maintaining the amorphous structure. In addition, the IGZO resistivity was largely tuned via varying the deposition conditions and the target composition.

Thereafter, Top-gate-staggered TFT devices with 40-nm-thick a-IGZO active layer were fabricated. LA with one pulse at lower energy densities (15 – 60 mJ/cm^2) provided TFT of improved performance. The optimised laser annealed TFTs (processed at 30 mJ/cm^2) exhibited an on/off ratio of 2.8 x 10^7, a field-effect mobility of 3.4 cm^2/Vs, a Von voltage of + 0.3 V, and a sub-threshold swing of 0.27 V/decade, compared to 6 x 10^6, 0.7 cm^2/V s, - 0.1 V, and 0.28 V/decade respectively for the as-deposited TFTs. This improvement in the TFTs transfer characteristics is attributed to reducing the resistivity of the channel layer (a-IGZO), and reducing the contact resistance between IGZO and the source/drain electrodes after processing.

LA at the reported energy density in this work is very promising for TFTs fabrication on heat sensitive plastic substrates. Moreover, since the required laser energy to enhance IGZO TFTs characteristics is rather low, a high throughput of IGZO-TFTs could be realised, making LA a promising technique for large volume production of large area electronics on flexible substrates.

Biography

Demosthenes C. Koutsogeorgis was born in New York, NY USA. He received his BSc in Physics from the University of Ioannina, Greece, in 1997, and his PhD in Materials Science from the Nottingham Trent University in 2003.
He has been a Lecturer at Nottingham Trent University since 2002 and in 2005 was promoted to Senior Lecturer. In 2013 he became a Reader in Photonic Technologies in the School of Science and Technology, at Nottingham Trent University. His research interests cover the fabrication and post deposition photonic processing of thin film materials for applications in plasmonics, electronics, optoelectronics and sensors.
Dr. D.C. Koutsogeorgis is a member of SID, OSA, E-MRS and MRS.

Panel Discussion

(W.5) Laser microfabrication in flexible electronics: what opportunities and how to scale up for mass market applications?

Moderator: Professor Bill O'Neill, Institute for Manufacturing, Department of Engineering, University of Cambridge

February 2016

1 - 2

POSTER SESSION

Robinson College, Cambridge
www.largeareaelectronics.org

Posters will be displayed in the exhibition hall near the registration area.

A drinks reception will be held in this same area on Monday 1st February from 18:10 -19:10, prior to the gala dinner.

The Programme Committee will award a prize to the best poster. This prize is generously supported by our Gold Sponsor.

NOVACENTRIX™

Poster presenters are requested to make sure that their poster is displayed on the appropriate board before lunch on Monday 1st and removed from conclusion of the lunch break on Tuesday 2nd.

POSTER SESSION

Poster	Title	Authors	Institution
P.1	Device Simulation of High Mobility Solution-Processed Transparent Oxide Quasi-Superlattice Transistors	Nikolaos A. Hastas, Yen-Hung Lin[1], Hendrik Faber[1], Thomas D. Anthopoulos[1]	[1] Department of Physics and Centre for Plastic Electronics, Blackett Laboratory, Imperial College London, London SW7 2AZ, United Kingdom
P.2	Device modelling of POSFET for large area touch sensing application	Shoubhik Gupta[1,2], Hadi Heidari1, Leandro Lorenzelli[2], Ravinder Dahiya[1]	[1] Bendable Electronics and Sensing Technologies (BEST) group, University of Glasgow, Glasgow, UK [2]Micro System Technology, Fondazione Bruno Kessler, Trento, Italy
P.3	Static force sensing enabled by P(VDF-TrFE) sensor coupled with organic thin-film transistor	Stuart Hannah[1*], Deepak Uttamchandani[1], Ravinder Dahiya[2] and Helena Gleskova[1]	[1]Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, G1 1XW, UK [2]Electronics and Nanoscale Engineering Division, School of Engineering, University of Glasgow, G12 8QQ, UK
P.4	Inkjet printing of ultrahigh sensitivity humidity sensors based on two-dimensional materials	Pei He[1], John R. Brent[2], David J. Lewis2, Paul O' Brien2 and Brian Derby[1*]	[1] School of Materials, University of Manchester, Oxford Road, M13 9PL, U.K [2] School of Chemistry, University of Manchester, Oxford Road, M13 9PL, U.K
P.5	Simulation Scenarios of Ultra-Thin Chips in Smart Large-Area Flexible Electronics	Hadi Heidari, Shoubhik Gupta, Ravinder Dahiya	Bendable Electronics and Sensing Technologies (BEST) group, Electronics and Nanoscale Engineering Division, University of Glasgow, Glasgow G12 8QQ, UK
P.6	The challenge of Systems Integration – a case study from the IEC	Alan Hodgson	Alan Hodgson Consulting
P.7	Hybrid transistors and integrated circuits processed from solution at low temperatures	Ivan Isakov, Alexandra Paterson and Thomas D. Anthopoulos	Imperial College London
P.8	Organic ring oscillators with sub-200 ns gate delay from a p-type semiconducting blend	D M Taylor[1], C P Watson[1,2], B A Brown[2], J Carter[2] and J Morgan[2]	[1] School of Electronic Engineering, Bangor University, Dean Street, Bangor, Gwynedd LL57 1UT, UK [2]SmartKem Ltd, Hexagon House, Delaunays Road, Blackley, Manchester M9 8GQ, UK
P.9	In Process Surface Metrology for Roll to Roll Manufacture of Ultra Barrier Film	Liam Blunt[1], Hussam Muhamedsalih[1], Mohamed Elrawemi1, Haydn Martin[1], Ivo Hamersma[2], Feng Gao[1], X. Jiang[1], David Bird[3]	[1]University of Huddersfield, UK [2]IBS Precision Engineering, Netherlands, [3]Centre for Process Innovation, Sedgefield, UK
P.10	Convective self-assembly, a versatile tool for nano-pinballing and ordering (semi)conducting/emissive nanoparticles and polymers on large areas	Ioan Botiz[1,2], Shengyang Chen[1] Paul Stavrinou[1], Natalie Stingelin[1]	[1]Imperial College London (UK) [2]Babes-Bolyai University (Romania)
P.11	Patterning strategies for integration of multifunctional organic/inorganic hybrid structures	Shengyang Chen, Ioan Botiz, Paul Stavrinou, Natalie Stingelin	Imperial College London
P.12	High Barrier for Plastic Electronics (HiBPE)	*Andrew G. Cook[1], Philip Hollis[1] Bob Jarman[2], James Shipman2, Mark Spratt[3], David Bird[1], *Paolo Melgari[1], Steve Edge1, Sam Chan[1], Alf Smith[1], Steve Spruce[1]	[1] The Centre for Process Innovation (CPI) Limited, Thomas Wright Way, NETPark, Sedgefield, TS21 3FG [2] Camvac Limited, Burrell Way, Thetford, Norfolk, IP24 3QY [3] G24Power Ltd, South Lake Drive,

			Imperial Park, Newport, NP10 8AS
P.13	Large Area Fabrication of micron scale metallic structures on photo paper substrates	M.D. Cooke, S.E. Trattles & D. Wood	School of Engineering and Computing Sciences, Durham University, South Road, Durham DH1 3LE
P.14	High-Speed Contactless Electrical Evaluation of Printed Electronics using Inductive Sensors	Adam Lewis*, Chris Hunt, Owen Thomas and Martin Wickham	National Physical Laboratory, Teddington, UK
P.15	Flexible Large Area OLED and OPV Devices Manufactured by Thermal Evaporation and Spin-coating, using Flexible ITO-free TCO Electrode	Paolo Melgari[1], (Sam) Yun Fu Chan[1], Phil Hollis[1], Parnia Navabpour[2], Kevin Cooke[2], Joanne Stallard[2], Sue Field[2], Alexander Goruppa[3], Katrin Zorn[3], Manuel Auer[4], Andreas Klug[4], Emil J.W. List-Kratochvil[4,5], Guosheng Shao[6]	[1]Centre for Process Innovation (CPI), Sedgefield, United Kingdom, [2]Teer Coatings Ltd, Miba Coating Group, Droitwich, United Kingdom, [3]High Tech Coatings, Miba Coating Group, Vorchdorf, Austria, [4]NanoTecCenter Weiz Forschungsgesellschaft mbH, Austria, 5Institute of Solid State Physics, Graz University of Technology, Austria, [6]University of Bolton, Bolton, United Kingdom
P.16	Effect of grain boundary position on the drain current of polysilicon source-gated transistors	Luke J Wheeler and Radu A Sporea	Advanced Technology Institute, University of Surrey, Guildford, GU2 7HX, U.K.
P.17	OPCAP: Offset lithographic printing of high-k dielectric capacitors	Professor Bob Stevens, Dr Neranga Abeywickrama, Dr Simon Thompson	Nottingham Trent University
P.18	Spray coated silver nanowires as transparent electrodes for printed PVs on opaque substrates	Vasil Stoichkov*, Dr Ziqian Ding, Dr Jeff Kettle	School of electronic engineering, Bangor University, Dean St., Bangor, Gwynedd, LL57 1UT, Wales, UK
P.19	Solution-Processed Co-planar Nano-Scale LEDs by Adhesion Lithography (a-Lith)	Gwenhivir Wyatt-Moon, Dimitra G. Georgiadou, James Semple, and Thomas D. Anthopoulos	Department of Physics and Centre for Plastic Electronics Imperial College London, Blackett Laboratory, London, SW7 2BW
P.20	Laser Direct Writing of RF Passive Components on Flexible Substrates	F. Zacharatos[1] N. Iliadis[2], J. Kanakis[2], P. Bakopoulos[2], H. Avramopoulos[2] and I. Zergioti1	[1] National Technical University of Athens, Physics Department, Heroon Polytehneiou 9, 15780, Zografou, Greece [2] National Technical University of Athens, School of Electrical & Computer Engineering, Heroon Polytehneiou 9, 15780 Zografou, Greece.
P.21	Development of a Method for the Manufacture of Hybrid Energy Storage Using 3D Printing Technology	Milad Areir*, Yanmeng Xu*, Eujin Pei, David Harrison, John Fyson, Anan Tanwilaisiri and Ruirong Zhang	Cleaner Electronics Group, College of Engineering, Design and Physical Sciences, Brunel University London, Uxbridge, UK
P.22	Energy Harvesting with Plastic Electronics	Stuart Higgins; Henning Sirringhaus	Optoelectronics Group, Cavendish Laboratory, JJ Thomson Avenue, Cambridge, CB3 0HE
P.23	Flexipower: Printed Radio Frequency Energy Harvesting	Tim Mortensen, Philip Cooper	Swansea University
P.24	Polymer-Sorted Semiconducting Single Walled Carbon Nanotubes for Next-Generation Flexible Nanoelectronics	F. Bottacchi[1], L. Petti[2], I. Namal[3], F. Späth[3], D. Georgiadou1, G. Tröster[2], T. Hertel[3], and T. D. Anthopoulos[1]	[1]Department of Physics and Centre for Plastic Electronics, Imperial College London, London, UK [2]Electronics Laboratory, Swiss Federal Institute of Technology, Zürich, Switzerland [3]Institute of Physical and Theoretical Chemistry, Julius-Maximilian University Würzburg, Würzburg, Germany

P.25	Stretchable, transparent and conductive graphene film	F. Torrisi[1], I. R. Minev[2], T. Carey[1] S. P. Lacour[2]	[1] Cambridge Graphene Centre, University of Cambridge, Cambridge CB3 0FA, UK, [2] École Polytechnique Fédérale de Lausanne, Centre for Neuroprosthetics, BM 5131, Station 17, CH-1015 Lausanne, Switzerland
P.26	Solution-processed, centimeter-sized, single-crystalline layers for high-performance organic thin-film transistors	R. Janneck[1,2], S. P. Bommanaboyena[1], F. T. Mehari[1], J. Genoe[1,2], P. Heremans[1,2], C. Rolin[1]	[1] IMEC, Large Area Electronics, Kapeldreef 75, B-3001 Leuven, Belgium [2] KU Leuven, ESAT, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium
P.27	High Mobility Solution-Processed Organic Small Molecule-Polymer Blend Thin-Film Transistors with Hole Mobilities of up to 13 cm^2/Vs	Alexandra F. Paterson, Weimin Zhang, Martin Heeney, Iain McCulloch, Neil D. Treat, Olga Solomeshch, Nir Tessler, Thomas D. Anthopoulos	Department of Physics and Centre for Plastic Electronics, Blackett Laboratory, Imperial College London, London SW7 2BW, United Kingdom
P.28	Transfer Printing Si Nanowires for Flexible Large Area Electronics	D. Shakthivel, W. Taube, C. Garcia Núñez, F.Liu, R. Dahiya*	Bendable Electronics and Sensing Technologies (BEST) Group, Electronics and Nanoscale Engineering (ENE), School of Engineering, University of Glasgow, G12 8QQ, UK
P. 29	Copper(I) thiocyanate (CuSCN) as a hole-transport layer material for large-area opto/electronics	Nilushi Wijeyasinghe*, Nir Yaacobi-Gross, Pichaya Pattanasattayavong and Thomas D. Anthopoulos	Department of Physics and Centre for Plastic Electronics Imperial College London, Blackett Laboratory, London, SW7 2BW (United Kingdom)
P.30	High resolution high velocity laser printing of metal lines	D. Puerto[1], E. Biver[2], A.-P. Alloncle[1] D. Karnakis[2], I. Zergioti[3], Ph. Delaporte[1]	[1]Aix-Marseille University, CNRS, LP3 laboratory Campus de Luminy, C.917, Marseille, France [2]Oxford Lasers Ltd., Unit 8, Moorbrook Park, Didcot, OX11 7HP, United Kingdom [3]National Technical University of Athens, Physics Department, Zografou Campus Greece, 15780
P.31	Digital Laser Thin Film Layer Patterning of Transistor Electrodes on Flexible Substrate	R. Geremia[1], N. Bellini[1], S. Norval[2], D. P. Hand[3], D. Karnakis[1] and G. Fichet[2]	[1] Oxford Lasers Ltd, Unit 8 Moorbrook Park, Oxfordshire, OX11 7HP, United Kingdom [2] FlexEnable Ltd, 34 Cambridge Science Park, Cambridge, CB4 0FX, United Kingdom [3] Heriot-Watt University, School of Engineering and Physical Science, Edinburgh, EH14 4AS, United Kingdom
P.32	Laser processing for P3-scribing on CIGS based solar cell	S. Leyder [1)*], G. Coustillier [1)], B. Dunne [2)], P. Delaporte [1)]	[1)] Aix-Marseille University - CNRS - LP3 Laboratory, 163 avenue de Luminy C.917, 13009 Marseille, France [2)] NEXCIS Photovoltaic Technology, 240 avenue Olivier Perroy, Rousset cedex, France
P.33	Fault-tolerant strategies for printed electronics	Richard McWilliam[1], Philipp Schiefer[1], Alan Purvis[1]	School of Engineering and Computing Sciences, Durham University, Science laboratories, South road, Durham, DH1 3LE, United Kingdom
P.34	Regioregular synthesis of accetor-functionalised oligothiophenes.[1]	Alan A. Wiles*[a], Brian Fitzpatrick[a], Niall A. McDonald[a], Mary Margaret Westwater[a], De-Liang Long[a], Bernd Ebenhoch[b], Vince Rotello[c], Ifor D. W. Samuel[b], Graeme Cooke[a]	[a]Glasgow Centre for Physical Organic Chemistry (GCPOC), WestCHEM, School of Chemistry, University of Glasgow, Glasgow, G12 8QQ, U.K.

			[b]Organic Semiconductor Centre, SUPA, School of Physics and Astronomy, University of St Andrews, North Haugh, St Andrews, Fife KY16 9SS, UK [c]Department of Chemistry, University of Massachusetts, Amherst, MA 01003, USA.
P.35	Roll to Roll Patterning of Thin Film Transistor Contacts	Thomas Cosnahan	Department of Materials, St Edmund Hall, Oxford University
p.36	Large volume continuous synthesis of metal oxide nanoparticle inks toward inkjet printed TFT devices	Sean Butterworth[1], Callum Crawshaw[1], Pete Gooden[1], Susanne Oertel[2] and Michael P. M. Jank[2]	[1]Promethean Particles Ltd, 6 Faraday Building, Nottingham Science Park, University Boulevard, Nottingham, NG7 2QP, UK [2] Fraunhofer Institute for Integrated Systems and Device Technology IISB, Schottkystr. 10, 91058 Erlangen, Germany

(P.1) Device Simulation of High Mobility Solution-Processed Transparent Oxide Quasi-Superlattice Transistors

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Thin-film transistors (TFTs) based on metal oxide semiconductors represent an emerging technology that promises to revolutionise large-area electronics due to the high carrier mobility, optical transparency, mechanical flexibility and the potential for low-temperature processing. The performance of TFTs depends strongly on the intrinsic properties of the active layer material and though it is limited by them. In order to overcome this limitation, low dimensional heterostructures based on transparent oxides grown have been fabricated using sequentially staggered layers of intrinsically or extrinsically doped materials. In these kind of structures, the majority carriers diffuse out from the extrinsically doped semiconductor to the undoped layer or at the interface between them and form a two-dimensional (2-DEG) electron gas. The confined electrons of the 2-DEG electron gas minimizes the ionized impurity scattering of the carriers and thus increase the mobility of the semiconductor which in many cases is higher than the mobility of the bulk semiconductor. This 2-DEG confinement layer can be used as an active channel for implementation of high mobility thin-film transistors.

Usually, the electron gas confinement layer imposes high quality heterointerfaces between the sequential grown layers and thus the experimentally observed devices have been fabricated by molecular beam epitaxy or other epitaxial techniques at relatively high temperatures and low pressure. A key challenge is to fabricate such electron confinement layers using simpler, scalable and cost-effective fabrication processes, which are compatible with low temperature substrate materials.

Here, low-dimensional polycrystalline quasi-superlattices (QSLs) consisting of alternating layers of In_2O_3, Ga_2O_3 and ZnO were grown by sequential spin casting and thermal annealing at temperatures in the range 180-200 °C. Three differentmultilayer oxide structures: a) heterojunctions between two different types of layers

(In_2O_3/ZnO, In_2O_3/Ga_2O_3, ZnO/Ga_2O_3); b) three-layer structures consisting of In_2O_3/ZnO/In_2O_3 (QSL-1) and In_2O_3/Ga_2O_3/ZnO (QSL-2); and c) superlattices In_2O_3/Ga_2O_3/ZnO/Ga_2O_3/In_2O_3 (QSL-3).

Device simulation of transfer and output characteristics has been implemented

based on surface potential analytical model in metal oxides. Determination of deep and tail states in the energy gap of the superlattices has shown that the interfaces between sequential layers play a significant role to the mobility enhancement and 2- DEG electron confinement between the layers. Simulation of transfer and output characteristics as a function of temperature reveals the transport mechanisms of electrons caused by the electron confinement in the interfaces and the mobility enhancement mechanism. Further work on band structure engineering could lead to the enhancement of localized electron confinement, increasing further the electron charge density and the mobility of superlattice structures.

Keywords: Device simulation, Superlattice transistor, Mobility, Deep states, Tail states

Biography

Nikolaos A. Hastas received the M.Sc. degree in Material Science (2000) and the Ph.D. degree (2004) on Microelectronics from Aristotle University of Thessaloniki (AUTH), Thessaloniki, Greece. He worked as a Post-Doc researcher from 2006-2015 in Micro- and Nano-Electronic Devices MiNED, AUTH, Greece. He currently works as a Research Fellow ("SUPERSOL", IF Marie Sklodowska–Curie 2014 project) in Advanced Materials and Devices (AMD) group, Imperial College London, UK. His current research interests include solution-processed materials growth and transparent oxide semiconductor device fabrication, electrical characterization and modelling of Thin Film Transistors (TFTs), diodes and transparent electronic devices.

(P.2) Device modelling of POSFET for large area touch sensing application

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In this paper, we reports the recent work related to the emerging area of piezoelectric oxide semiconductor field effect transistor (POSFET) based touch sensing system for the application in electronic skin. In POSFET device we take the advantage of piezoelectric polymer poly[(vinylidenefluoride-co-trifluoroethylene] (PVDF-TrFE) 's property of converting mechincal stimulus to electric charge and then couple it with a MOSFET, as evident from Fig.1, which leads

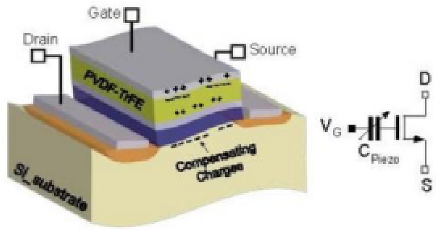

Fig 1: POSFET device structure and its schematic circuit symbol

to many advantages like better integration, spatial resolution, less signal to noise ratio and compatibilty with IC industry[1].

We propose a novel model for this device which shows how the piezoelectric properties of polymer affects the flow of charge in the channel region of underlying transistor. By combining the ferroelectric capacitor model with standard MOS physics, we can see the effect of poling (aligning of dipoles by applying high voltage acrross the polymer film) on the charge distribution in semiconductor region[2].

$$I_{DS}\begin{cases}\mu_n C_{stack}\left(\frac{W}{L}\right)\left\{\left(V_{gs}-V_{th_{eff}}\right)V_{ds}-\left(\frac{1}{2}\right){V_{ds}}^2\right\} & Linear \\ \mu_n C_{stack}\left(\frac{W}{L}\right)\left\{\left(V_{gs}-V_{th_{eff}}\right)^2\right\} & Saturation\end{cases} \quad (1)$$

Where, $V_{th\_eff} = V_{th} - \left(\frac{P_s+P_r}{C_{ox}}\right)$ (2)

and $\frac{1}{C_{stack}} = \frac{1}{C_{ox}} + \frac{1}{C_{PVDF}}$ (3)

Here, W/L is aspect ratio, un is electron mobility, Cox is oxide capacitance, CPVDF is polymer capacitance, Ps is saturation polarization and Pr is ramnent polariation.

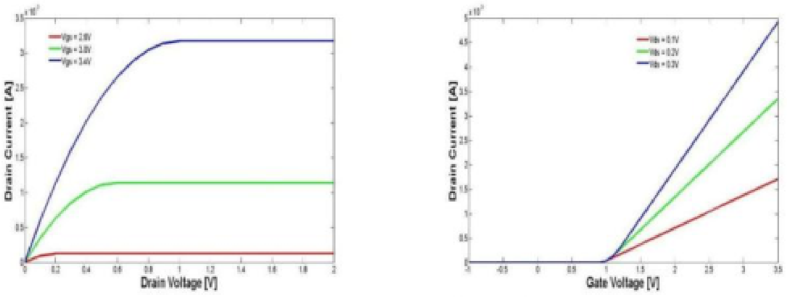

Fig. 2: Drain Current as a function of (left) Drain voltage (right) Gate voltage.

[1] R. S. Dahiya, A. Adami, L. Pinna, C. Collini, M. Valle, and L. Lorenzelli, "Tactile Sensing Chips With POSFET Array and Integrated Interface Electronics," *Sensors Journal, IEEE,* vol. 14, pp. 3448-3457, 2014.

[2] S. L. Miller, R. D. Nasby, J. R. Schwank, M. S. Rodgers, and P. V. Dressendorfer, "Device modeling of ferroelectric capacitors," *Journal of Applied Physics*, vol. 68, pp. 6463-6471, 1990.

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Leandro Lorenzelli received his Ph.D. degree in Electronics Materials and Technologies from University of Trento, Trento, Italy, in 1998. In 1998, he joined the Microsystems Division at the Fondazione Bruno Kessler, Center for Materials and Microsystems (FBK-CMM), Trento. His main research interests are on technologies for lab-on-a-chip for agro-food applications, smart lens, and more recently, paper-based microfluidics.

Ravinder Dahiya received the Ph.D. degree from the Italian Institute of Technology, Genoa, Italy. He is a Reader in Electronics and Nanoscale Engineering at the University of Glasgow, Glasgow, U.K. His research interests include flexible and printable electronics, tactile sensing, electronic skin, and robotics.

(P.3) Static force sensing enabled by P(VDF-TrFE) sensor coupled with organic thin-film transistor

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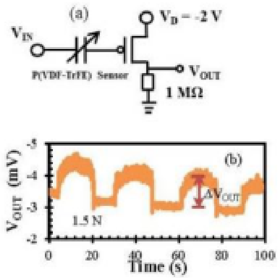
The ability to accurately monitor applied force has gained increasing momentum in recent years, particularly for the development of large-area robotic and/or electronic skin. While several technologies have been explored at present, the combination of flexible pressure sensors with organic circuitry can satisfy the growing demand for low-cost, large-area, flexible, rollable, and stretchable sensor circuits. The most common flexible and stretchable sensing modes are resistive[1] and capacitive[2], although piezoelectric[3] was also demonstrated.

The pressure sensor presented here utilises ferroelectric copolymer polyvinylidene fluoride-trifluoroethylene (P(VDF-TrFE)) which can be exploited for capacitive and piezoelectric sensing to detect static and/or dynamic forces. The parallel-plate sensor consists of a 2.5-µm-thick P(VDF-TrFE) layer sandwiched between Al and Au electrodes with an active sensing area of 25 mm^2. As shown in Figure 1(a), the sensor was connected to the gate electrode of a low-voltage p-channel organic transistor based on dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT)[4] with channel length of 30 µm and channel width of 1 mm. At present, normal compressive force was applied to the sensor to modify its capacitance, however future work will also exploit the piezoelectricity of P(VDF-TrFE). The force was applied across 40% of the sensor area.

Figure 1(b) shows the output voltage V_{OUT} when a force of 1.5 N is repeatedly applied to the sensor. The applied force changes the sensor's capacitance that is coupled to the gate of the organic transistor, resulting in a change in the transistor drain current. Various input voltages (V_{IN}) were chosen to study the response of the sensor circuit to static force. Figure 2 shows the effect of applied force on the change in V_{OUT} of Figure 1(a) for three values of V_{IN}. As the compressive force increased from 0 to 7.12 N, $|\Delta V_{OUT}|$ increased linearly with the applied normal force for all three V_{IN} values, with the highest sensitivity of 1.54 mV/N seen for $V_{IN} = -2$ V. In our experimental setup the force of 1 N translates to compressive pressure of about 83 kPa. Since the sensory requirements for tactile skin range from 1 to ~1000 kPa, the proposed pressure sensor is promising for tactile robotic skins.



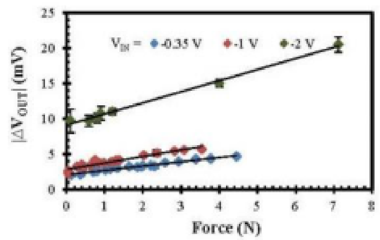


Fig.1 (a) Sensor circuit; (b) Force of 1.5 N applied repeatedly. Fig.2. $|\Delta V_{OUT}|$ versus force for V_{IN} = −0.35, −1 and −2 V.

1. T. Sekitani, U. Zschieschang, H. Klauk and T. Someya, *Nature Materials*, 2010, **9**, 1015.
2. I. Graz, M. Kaltenbrunner, C. Keplinger, R. Schwödiauer, S. Bauer, S. Lacour and S. Wagner, *Appl. Phys. Lett.*, 2006, **89**, 073501.
3. C. Dagdeviren, Y. Su, P. Joe, R. Yona, Y. Liu, Y. Kim, Y. Huang, A. Damadoran, J. Xia, L. Martin, Y. Huang and J. Rogers, *Nature Communications*, 2014, **5**, 4496.
4. S. Gupta, S. Hannah, C. Watson, P. Sutta, R. Pedersen, N. Gadegaard and H. Gleskova, *Org. Electronics*, 2015, **21**, 132.

Biography

Stuart Hannah received the BEng (Hons) degree in Electronic and Electrical Engineering from the University of Strathclyde, Glasgow in 2013. He is currently studying towards a PhD in Electronic and Electrical Engineering at the University of Strathclyde, which is funded by an EPSRC Doctoral Training Grant. He is a student member of the Institution of Engineering and Technology (IET) and the Royal Society of Chemistry (RSC). His research interests include organic thin-film transistors; sensor systems for detection of contact pressure and temperature, and flexible, large-area electronic/robotic skins.

(P.4) Inkjet printing of ultrahigh sensitivity humidity sensors based on two-dimensional materials

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Detecting and controlling of environmental moisture levels is of paramount importance for semiconductor industry, medical applications, food processing, and human activities. Various types of materials have been used as humidity sensors over the decades. Generally, an ideal humidity sensor requires high sensitivity, wide humidity detection range, as well as quick response and short recovery time. As is known, the sensitivity of humidity responsiveness normally relies on the exposure area of sensing materials to moisture molecules. Thus, to achieve high sensitive, materials with large specific surface area are required.

Graphene, a two-dimensional of one carbon atom thick exhibiting high surface area and exceptional electrical properties, owns great potential for ultrasensitive detection. High sensitive gas sensors based on graphene have been widely investigated in last several years. However, for moisture detecting, pristine graphene shows low sensitive due to the absence of functional groups and defect sites. Alternatively graphene oxide (GO), a graphene derivative, presents great advantages as a humidity sensing material. GO is not only a 2D honeycomb structure of carbon atoms, but also contained with oxygen functional groups, such as hydroxyl, carboxyl, and epoxy groups. These functional groups can react with water molecules and generate protons, leading a decrease in electrical impedance. Hence, the interaction of GO with molecules can be used in humidity sensing applications. Moreover, GO can disperse in water to form stable inks. This makes it suitable for low-cost solution process, such as inkjet printing.

Herein, we show a humidity sensor using GO as the sensing material by fully inkjet printing. The GO-based sensors exhibit ultrahigh sensitivity, as well as short response and recovery times. The humidity sensitivity of the GO sensors showed a sensitive of 4.45×10^4 times in capacitance 97% relative humidity (RH). The response and recovery time of the GO sensors are 6.5 s and 1.8 s, respectively. Moreover, the same concept has also been investigated in the case of other 2D materials, such as solvent exfoliated few-layer black phosphorus (BP). The BP-based humidity sensors showed a sensitive of 5×10^3 times with a response time of 5.4 s and recovery time of 2.1 s. The ultrasensitive and fast response and recovery speed of these sensors allow us to use them as a non-contact control interfaces by finger tips. We believe that the unique properties of 2D materials combine with inkjet printing technique may result good opportunity for low-cost applications in various fields such as flexible electronics.

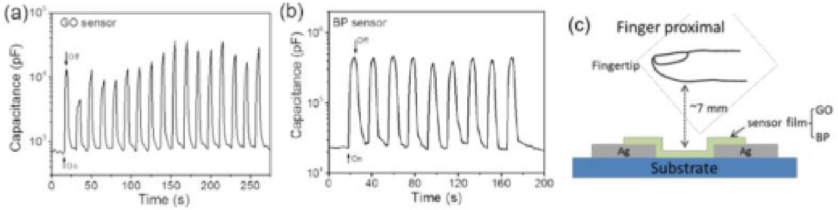

Figure 1. Time-resolved dynamic tests of the sensing response on the near distance of a fingertip proximal under ambient air condition, defined as finger 'on' and 'off' states, (a) GO sensor and (b) BP sensor. (c) The schematics of a fingertip approaching the fully printed sensor.

Biography

Pei He graduated from Xidian University with a BEng in Telecommunication Engineering, China, in 2009. Then he studied in organic electronic devices at Shanghai Jiao Tong University under the supervision of Prof. Xiaojun Guo and obtained his MEng degree in Electronic Engineering, in 2012. He started the PhD program in nanostructured materials at the University of Manchester under the supervision of Prof. Brian Derby since September, 2012. His research now is focused on inkjet printing of graphene-based two dimensional materials for electronic applications.

(P.5) Simulation Scenarios of Ultra-Thin Chips in Smart Large-Area Flexible Electronics

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Smart Large-Area Electronics (LAE) needs to be flexible and use high-performance computation front-end system. Despite all successes in flexible organic sensing devices, conventional CMOS ICs have efficient functionality for sensor interface circuits, communication, and embedded computation. Therefore, the architectures that combine LAE and CMOS ultra-thin ICs, can leverage the strengths of both technologies to enable sensing along with these functions[1]. However, the most challenging part of this combination is prediction of the bending stress effects on bendable ICs. Because bending stress changes the transistor characteristics such as current-voltage or drain-current variation and threshold-voltage shift. Furthermore, the interconnections between two technology, ~~of~~ LAE and ultra-thin ICs to transfer analog and digital signals for computation processing is key limitation. This issue is handled through contactless

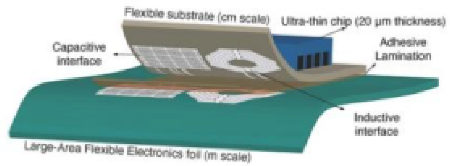

Fig.1: Illustration of ultra thin chip over flexible substrate with inductive and capacitive interface

interfacing by using capacitive and inductive antennas[2], as shown in Fig. 1.

In order to fabricate ICs that function within specifications, both planar as well as during mechanical deformation, the effects of stress must be considered in the design process. Modelling of bendable devices will play a critical role in design of bendable ICs and will help to produce cost-effective and reliable flexible electronics, which have different simulation scenarios in both, SPICE (Simulation Program with Integrated Circuit Emphasis) and FEM (Finite Element Method). The conventional complementary- metal-oxide-semiconductor (CMOS) transistor compact models for SPICE simulations can predict the response of devices produced via various standard technologies. The local-induced stress-effects have been intensively studied and included in device compact models. On the other hand, the effects of externally-induced stress are under investigation and the existing compact models are inadequate for electronics over flexible and bendable substrates. This abstract addresses this limitation of conventional circuits simulation tools by providing a new CAD-based simulation flow that include the bending (both static and dynamic) related effects on device behaviour, as shown in Fig. 2. Effects of deformation such as static and dynamic bending of the bendable substrates with electronics over them will be accounted for. The new model will allow early prediction (i.e. during the design phase itself) of the bending related effects in the electrical behaviour of devices and empower us to design circuits capable of operating reliably during arbitrary deformations. By using such flows, any change of the electrical parameters of transistors induced by deformation can be predicted in the early phase of the schematic design in SPICE simulators such as Cadence environment.

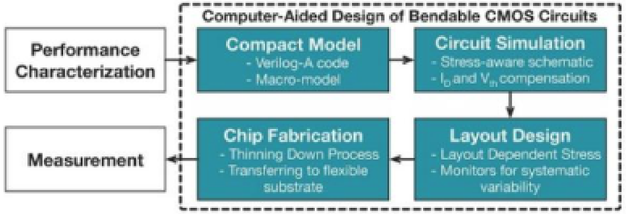

Fig.2: A CAD-based simulation flow to study electrical device characteristics of bendable CMOS integrated circuit.

[1] Verma, Naveen et. al "Enabling Scalable Hybrid Systems: Architectures for exploiting large-area electronics in applications." *Proceedings of the IEEE* 103, no. 4 (2015): 690-712.
[2] Hu, Yingzhe, et al. "Large-scale sensing system combining large-area electronics and CMOS ICs for structural-health monitoring." Solid-State Circuits, IEEE Journal of 49.2 (2014): 513-523.

Author Biographies

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Shoubhik Gupta received his bachelor degree from IIT Kanpur in 2014 and working on his doctoral research in Bendable Electronics and Sensing Technology (BEST) group at University of Glasgow. His area of interest lies in flexible electronics and semiconductor physics.

Ravinder Dahiya received the Ph.D. degree from the Italian Institute of Technology, Genoa, Italy. He is a Reader in Electronics and Nanoscale Engineering at the University of Glasgow, Glasgow, U.K. His research interests include flexible and printable electronics, tactile sensing, electronic skin, and robotics.

(P.6) The challenge of Systems Integration – a case study from the IEC

Alan Hodgson

Alan Hodgson Consulting

It looks unlikely that devices made wholly from printed, plastic, organic and flexible electronics is the way forward for industrialisation. Some level of systems integration looks likely to be needed to facilitate this. That then leaves open the question of how to best guide research communities to address these challenges.

This paper proposes a route to gather data to inform this debate by tapping into the collective wisdom available from the work of the International Electrotechnical Commission (IEC). As the IEC exists to produce "International Standards and Conformity Assessment for all electrical, electronic and related technologies" it covers the whole of the systems space into which Large Area Electronics could feasibly integrate.

The work of the IEC is divided up into individual Technical Committees to provide some structure to this wide area. Each of these Technical Committees gathers an international group of experts to guide the work into areas of industrial relevance. As such a glance at the work packages and roadmaps of the Technical Committees provides an important consensus overview that can guide groups such as research consortia into directions of relevance.

These Technical Committees do not work in isolation. The IEC provides for liaison structures between other IEC and ISO Technical Committees and external trade organisations. This is important as it provides both a route to manage overlap areas but also to address the challenge of systems integration that would cover the work of multiple Technical Committees.

The IEC also has one further level of initiatives that guide systems integration. The Standardization Management Board that oversees the work of the Technical Committees commissions special initiative in areas that require significant levels of integration across multiple technologies. Recent initiatives include Smart Cities and Wearable Smart Devices.

In 2012 the IEC set up Technical Committee 119 to bring the area of Printed Electronics into these systems. Since then IEC TC119 has created an international network of over 100 experts, evolved a roadmap to guide the work and created a liaison network across other Technical Committees and external organisations.

This paper will provide an overview of the ecosystem that has grown up around IEC TC119 with a focus on the guidance that this may provide on the worldwide interest in systems integration for printed, plastic, organic and flexible electronics. The geographic mix, proposed International Standards, genesis of test methods for lifecycle assessment, roadmap and liaison strategy will all be covered, together with an update on the ISO/IEC Wearables debate.

Biography

Alan Hodgson has had practical involvement in the production of International Standards for over 10 years. He has been Chair of IEC TC119 from first formation and has thus seen the evolution of the above areas.
He has practical experience in the area of Large Area Electronics and the systems integration space through a 2-year project within 3M, utilising production printing presses to make features for evaluation within the wider 3M manufacturing space.
Alan has recently returned to his consultancy business and is a Visiting Academic at the Centre for Digital Fabrication within the University of Manchester.

(P.7) Hybrid transistors and integrated circuits processed from solution at low temperatures

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Metal oxide and organic-based thin-film transistors (TFTs) are rapidly becoming the new building blocks in the emerging field of large-area, printable microelectronics. This is primarily due to the fact that the two families combine unique physical properties such as high charge carrier mobility and optical transparency with superior mechanical flexibility. Unlike organics, metal oxides have only recently shown to be compatible with inexpensive and temperature-sensitive substrates such as plastic paving the way to a host of exciting new applications that could well complement those based on their organic counterparts. Unfortunately, to date, the development of microelectronics based solely on organics or metal oxides is not practical enough primarily due to predominantly unipolar nature of best performing materials available, which in turn restricts their use in unipolar logic circuits that are known to be associated with numerous disadvantages. To this end, complementary logic technology (also known as CMOS) can provide a solution towards large-scale circuit integration. This however often comes at a cost in terms of manufacturing complexity since complementary technology relies on the combination of electron transporting (n-type) and hole transporting (p-type) semiconductors.
Here we report the development of hybrid organic-inorganic TFTs and simple logic circuits based on the combination of p-type organics and n-type metal oxide semiconductors. Different metal oxide layers were investigated and deposited from solution at temperatures below 200 °C in air. Similarly, different solution-processable organic semiconductors were investigated as the p-type materials. Optimized systems exhibited high hole and electron mobility values typically in the range of 5-13 cm^2/Vs. Hybrid devices were then prepared by stacking the metal oxide and organic films to form a spatially separated ambipolar hetero-junction layer which was then incorporated into suitably designed device architectures. In these device structures, the gate geometry defines the operating character of the device (n-type or p-type), allowing for facile integration of p-type and n-type devices into functional logic circuits with minimum manufacturing complexity. Planar complementary inverters were also prepared by patterning organic and metal oxide semiconductors of matching carrier mobilities. These inverters showed high gains and negligible hysteresis.

Biography

Dr Ivan Isakov obtained his MSc degree in physics and electronics of semiconductors from St. Petersburg State University in 2011. He then joined London Centre for Nanotechnology at University College London to do PhD on the oxide semiconductor nanostructures. Ivan is currently working at Imperial College London in the group of Professor Thomas Anthopoulos. His research interest include solution processed metal oxide and organic thin film transistors, hybrid logic devices, integration and patterning techniques for high performance low cost electronics.

(P.8) Organic ring oscillators with sub-200 ns gate delay from a p-type semiconducting blend

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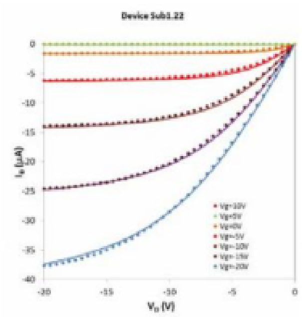
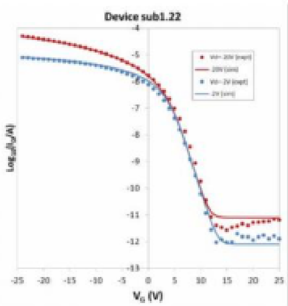
Abstract

This presentation will report the development of a process for fabricating organic ring oscillators with stage delay less than 200 ns. The active semiconductor is a p-type semiconductor ink (Tru-Flex® SKL09) based on a high mobility pentacene derivative formulated with an amorphous polyarylamine binder. Morphological studies suggest that after spin-coating onto the source-drain electrodes, the blend phase-separates to yield a thin upper layer enriched with the small molecule and comprising a uniform distribution of randomly orientated small crystallites, typically a few microns in size. Bottom-contact top- gate transistors were completed using a spin-coated film of Cytop® as the gate dielectric. Transistor parameters for subsequent circuit design and simulation were extracted using the Silvaco UOTFT model to fit transfer and output characteristics of devices with 4.6 □m channel length and channel widths ranging from 60 to 2160 □m. An example fit is shown in Fig.1.





Hole mobilities were typically in excess of 2 cm^2/Vs, threshold voltage ~4.5 V with on-off current ratios approaching 10^8. Depletion load (V_{GS}=0) inverters operating from a 20 V rail displayed excellent voltage transfer characteristics with gain of ~6 and noise margin ~2 V. Both experimental measurement and simulation showed that inverters were capable of MHz operation. Over 120 ring oscillators of various geometric designs were fabricated and yielded operational frequencies ranging from ~200 kHz to ~530 kHz. These correspond to stage- delays from ~500 ns down to ~190 ns, which are amongst the shortest reported for unipolar, solution-processed p-type organic semiconductors.

Key words: High-performance semiconducting blends, transistors, inverters, ring oscillators, simulation

Biography

Professor Taylor has led organic electronic research in the School of Electronic Engineering at Bangor University for 25 years. During this period he has built extensive fabrication, surface analysis and electrical measurement facilities for organic electronic devices and circuits. He has published widely on the use of admittance spectroscopy for investigating interfaces in metal-insulator-organic semiconductor structures. He has collaborated with researchers in many European countries, and in Japan and Brazil. His recent collaboration with Oxford and Manchester Universities has resulted in the development of an all-vacuum approach for the fabrication of organic electronic circuits. He has also undertaken Knowledge Transfer Partnerships with SmartKem Ltd, working with the company to validate a range of new, high-performance solution-processable semiconducting organic inks. Results from this collaboration will be reported at the meeting.

(P.9) In Process Surface Metrology for Roll to Roll Manufacture of Ultra Barrier Film

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Abstract

Increasing the yield of Roll to Roll manufacture of nano-scale thin film layers faces a major challenge of developing in-line detection micro/nano-scale defects on films surfaces. To date metrology systems capable of this task have yet to be fully developed where their robustness to the manufacturing environment is demonstrated. This paper introduces wavelength scanning interferometer (WSI) system developed as part of EU funded NanoMend project. The system comprises a full in line solution for inspection of entire surface regions of Roll to Roll substrate surfaces. The present paper introduces the application of the WSI to detect defects during Roll to Roll production of ultra barrier films for incorporation into flexible PV modules. Aluminium oxide, Al_2O_3, Atomic Layer Deposition (ALD) produced coatings are used as barrier layers for photovoltaic (PV) solar modules where the primary function of the barrier layer is to prevent the water vapour ingress to the PV cells and the target value for water vapour transmission (WVTR) is <1x10-4 g/m2/day at $35^{\circ}C$, 90%RH. Barrier layer defects have been shown to have negative impact on the performance of the barrier films' layers allowing increased WVTR through the barrier causing electrical shunts resulting in reduced PV module efficiency and lifespan. Based on extensive experiment and testing it was found that the WVTR performance of barrier films is dominated by defect where the lateral dimension exceeds 3 um. Consequently for optimum efficiency the defect detection system should be capable of measuring such defects. The metrology solution principle which capture surface topography is based on implementing an opto-mechanical in-process inspection system to measure and catalogue the significant film defects using a wavelength scanning interferometer (WSI) embedded within a film-rewinder stage and integrated with the substrate translation and kinematic stages. The metrology system additionally allows surface measurement over full substrate widths of approximately 0.5 m. To achieve this, the system has an auto-focus ability for the WSI with an accuracy and repeatability better than 6 µm at optimum optical alignment conditions. The opto-mechanical system has no mechanical movement and the consequent measurement time required for each area of captured data is less than 1 sec. To ameliorate external vibrations the measurement solution combines a dual path interferometer and a non-contact film holding capability. The paper also introduces the successful application of the WSI in a roll to roll environment and has provided evidence for the development of a commercial metrology system.

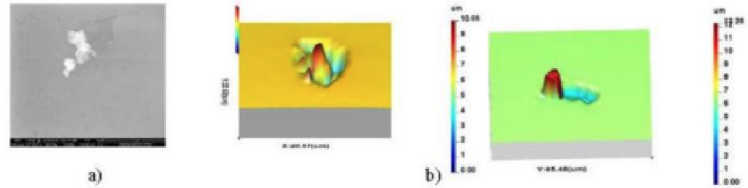

Figure 1 a) SEM of typical barrier film defect b) defects measured using the WSI in situ coated film measurement

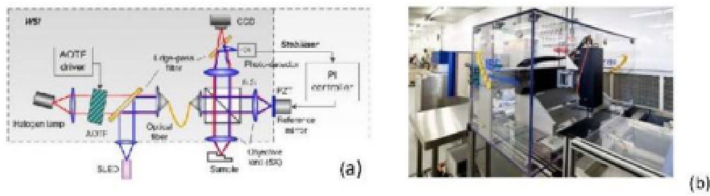

Figure 2 a) Schematic illustration if WSI system and b) deployed demonstrator

Biography

Professor Liam Blunt has an Hons degree in Materials Technology and a PhD from Coventry University. His Academic experience includes Post Doctoral periods at Warwick University and Birmingham University Whilst at Birmingham he developed an interest in tribology and surface metrology. In 1997 Prof Blunt moved to Huddersfield University and began developing the Centre for Precision Technologies CPT Prof Blunt has formed extensive industrial collaborations in particular with Amatek Taylor Hobson and held the Taylor Hobson Chair of Surface Metrology 2002-2012. He is currently Director of the CPT.

(P.10) Convective self-assembly, a versatile tool for nano-pinballing and ordering (semi)conducting/emissive nanoparticles and polymers on large areas

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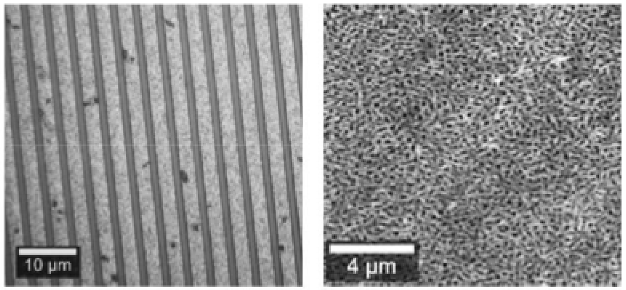
Abstract:

Convective self-assembly (CSA) is a method that can be used for nano- pinballing process by depositing, in a controlled manner, nano- to micro-sized colloids onto a surface relief structure under the action of solvent evaporation and capillary forces. By controlling various physical parameters, a large variety of structures can be obtained from different kinds of colloids, including conducting/emissive nanoparticles (left Figure). Furthermore, we show that CSA method can also be adapted to polymer solutions by controlling the deposition speed, substrate temperature and polymer concentration. Therefore, CSA leads to thin films comprised of molecules possessing highly oriented chain conformation over large areas (i.e. squared centimetres), including ordere/porous films and/or random nanoparticles of polyfluorenes and oligothiophenes (right Figure). The optoelectronic properties of resulting ordered structures are visibly changed in comparison to spin casted films of the same material that adopts a rather disordered microstructure.



CSA performed on 0.2 µm gold nanoparticles (left) and on oligothiophenes (right).

Keywords: convective self-assembly, nano-pinballing/ordering, nanoparticles, polymers

Biography

Dr. Ioan Botiz was a Marie Curie fellow at Haute Alsace University and received, in 2007, his PhD in Polymer Physics. He moved in 2008 to Argonne National Laboratory and focused on structuring of photovoltaic active layers and fabrication of organic energy devices. He was a FRIAS excellence postdoctoral fellow at University of Freiburg (2010-2013) working to understand the structure-property relationships in conjugated polymers. Since 2014 he is Research Associate at Imperial College London and Research Assistant at Babes-Bolyai University.

(P.11) Patterning strategies for integration of multifunctional organic/inorganic hybrid structures

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Abstract
Cross-cutting approaches, where molecular engineering and clever processing are synergistically coupled, allow chemists to tailor complex hybrid systems of various shapes with perfect mastery at different size scales, composition, functionality, and morphology. Hybrid materials with organic/inorganic or bio–/inorganic character represent not only a new field of basic research but also, via their remarkable new properties and multifunctional nature, hybrids offer prospects for many new applications in extremely diverse fields. This potential of hybrid materials is reflected by the fact that many of them are entering a variety of markets. In many cases, hybrid materials are constituted by organic components (molecules) or networks (organic polymers) intimately mixed at the molecular or nanoscopic level with inorganic components, such as metal oxides and metals, metallo-polymers but also phosphates, carbonates, chalcogenides and such derivatives. However, currently, most hybrid materials that find applications in industry are based mostly on the association between metallic and/or ceramic matter, frequently combined with organic molecules or 'plastics' of all kinds including bio-components. Here, I will present recent activities to design and develop novel strategies towards highly simplified, robust processing of self-assembled, multifunctional arrays at high yield. I will demonstrate procedures towards self-assembly and patterning of various functional species, including inorganic semiconductors such as ZnO, light-emitting quantum dots, or conducting and/or magnetic nanoparticles (e.g. Au, Cu, Co), with the use of surface relief structures and surface energy patterning strategies to create functional architectures at predefined locations without the need for any lithography steps. The key goal will be to produce a wide range of devices from p-n junctions, photovoltaic cells, electrode arrays with an unprecedented ease of processing without the need for lithographic methods and with a versatility to structure wide-range of inorganic (and inorganic/organic hybrid) materials.

Keywords: hybrid materials, patterning, surface relief structure, nano-pinballing

Biography

Shengyang Chen graduated from the Beijing University of Chemical Technology with a first class B.Eng. in Polymer Science and Engineering in 2014. His postgraduate study was carried out in Advanced Materials Science and Engineering in Imperial College London where he obtained a Distinction MSc degree. In 2015, he was awarded with Chinese Scholarship Council Scholarship and enrolled in the 4-year Plastic Electronics CDT programme. Now he works with Prof Natalie Stingelin and Dr Paul Stavrinou and his research project mainly focuses on exploiting patterning strategies for integration of multifunctional organic/inorganic hybrid structures; the use of additives for solution processing of phOLEDs and electrochromic active layers.

(P.12) High Barrier for Plastic Electronics (HiBPE)

***Andrew G. Cook[1], Philip Hollis[1], Bob Jarman[2], James Shipman[2], Mark Spratt[3], David Bird[1], *Paolo Melgari[1], Steve Edge[1], Sam Chan[1], Alf Smith[1], Steve Spruce[1]**

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Other Partners: Inside2Outside Ltd, SPECIFIC, Tata Steel Europe Ltd

Keywords
Roll–to–Roll (R2R), Atomic Layer Deposition (ALD), Barrier, Water Vapour Transmission (WVTR), Vacuum.

Abstract

HiBPE is a collaborative research and development project funded by Innovate UK, that aims to develop a low cost production route for the manufacturing of high performance ultra-barrier materials used for applications such as thin film inorganic, organic and dye-sensitized solar cells (DSSC), flexible solid state lighting (OSSL) and bendable display screens.

The aim of the 3 year project which began in 2013 is to produce high barrier film with a water vapour transmission rate of <5 x 10^{-4} g/m^2/day at a significantly lower cost than those currently available on the market. The processes developed will be compatible with in-line, all vacuum based deposition processing, suitable for inclusion in a roll to roll production machine, which would be scalable to commercial material widths (1m+) and production line speeds. Atomic Layer Deposition (ALD) has been highlighted as a potential technology to achieve this goal.

The poster will present details of the progress made within the project to date. An organic coating system, adapted from Camvac's technology, has been retrofitted to a conventional roll-to-roll sputter coating tool to investigate processing at line speeds associated with ALD. CPI has invested in a roll to roll tool to produce front sheet barrier film on 500mm wide film. Barrier films produced will be integrated with DSSC's modules at G24Power and OSSL's devices at CPI.

Biography

At CPI my main responsibly is process development on both the R2R ALD and R2R sputter coater. Prior to joining CPI, I worked at Oxford University in the Materials Department as part of the vacuum processing team. Main focus of the work undertaken was the production of **high energy density capacitors by roll to roll vacuum processing.** I gained a PhD in Chemistry from Aberdeen University, where I synthesised and characterised liquid crystal molecules. Continued working on liquid crystal materials at Halle University (Germany), primarily focused on dendritic systems as part of an EU funded multi-partner collaboration.

(P. 13) Large Area Fabrication of micron scale metallic structures on photo paper substrates

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Silicon is the industrial standard substrate for devices made using photolithographic processing. However, the use of flexible substrates, particularly plastics, has become more interesting commercially due to both the range of new devices possible and the potential to integrate the fabrication with print lines [1]. However, the cost of these flexible films still tends to be relatively high due to the specialist coatings needed to make the films stable against temperature and humidity changes.

Recently, there has been a drive towards using paper as a substrate material [2]. This has advantages in that paper is significantly cheaper, more environmentally friendly and will truly integrate with print lines when compared to plastic substrates. However there are certain disadvantages, the main ones being that using print technology limits both the minimum feature size and the range of available materials. Whilst this is satisfactory for many applications, in order to develop devices that are smaller and/or faster than is currently possible, it is desirable to be able to process smaller features of the order of 1 micron or less [3].

Presented here is a novel process which allows fabrication of micron scale features using a modified photolithographic technique. We demonstrate the use of the process to make structural changes to the surface topography in both negative and positive resists. Further to this, we show the capability of the process to pattern metal thin films to produce micron scale features which exhibit good electrical properties suitable for device fabrication.

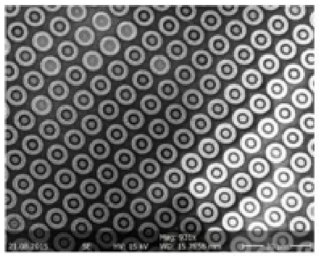

Figure1: Typical corbino electrode structures fabricated on paper

Clearly, in order to make it to market, it is essential that the process is both scalable and compatible with current equipment sets and process lines. We demonstrate how our process can be potentially integrated into roll to roll coating equipment and provide excellent uniformity and yield. A typical set of gold electrodes fabricated on a photo paper substrate are shown in figure 1.

References

[1] MacDonald W *Latest Developments in Polyester Film for Flexible Electronics* Dupont Teijin Films (2009) (http://people.ccmr.cornell.edu/~cober/mse542/page2/files/Barriers.pdf)

[2] Shenton SA, Cooke MD, Racz Z & Wood D. *Optimum fabrication methods and substrates for paper-based electronics* EMRS spring meeting, paper BB.VII-4 (11th-15th May 2015)

[3] Cooke MD, McCall KL, Bird DP, Lee YU, Pease T, Chan SYF, Palumbo M, McGloin S & Ogier SD, *OTFT Backplanes for Integration into Flexible Displays* Proc. SPIE Organic Field-Effect Transistors IX, 777814 (August 17, 2010)

Keywords: Paper, flexible, photo-lithography, electrodes, devices

Biography

Dr Michael Cooke is an experienced device fabrication scientist with a background in novel micro/nano devices and processes, organic / inorganic devices and magnetic device structures. He has experience in both industry and academia with a good understanding of the requirements of both sectors. Previously he worked at the CPI/PETEC Facility as a senior scientist and has detailed understanding of the requirements for process scale up. Currently Dr Cooke works as the Experimental Officer for the MEMs Facility within the School of Engineering and Computing Sciences at Durham University, working on a variety of projects including work with other institutes, SMEs and large multinationals. The facility has a full range of equipment sets from atomic layer deposition, nanoimprint lithography, electron beam lithography and metal layer deposition and photolithographic patterning as well as significant experience in device design and testing. All of which can be accessed by clients to allow flexible development of processes and devices.

(P.14) High-Speed Contactless Electrical Evaluation of Printed Electronics using Inductive Sensors

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National Physical Laboratory, Teddington, UK

Abstract

The market growth of conductive inks for flexible and printed electronics is predicted to increase from $2.3 billion to $3.2 billion by 2025[1]. It is important that we are able to verify the electrical properties of printed electronics to maintain output quality and reduce wastage. Therefore we are driven to find a suitable non-contact technique suitable to measure the electrical properties of the printed structures during manufacture in a roll-to-roll process. The emphasis of the work reported here is to use inductive sensors to measure electrical response. The impedance of an inductive sensor is affected by eddy currents induced in nearby conductors such that the electrical loss will be increased. The electrical response will be affected by a number of factors including material resistivity and thickness, temperature and sensor lift-off (distance between sample and sensor). By controlling temperature and lift-off we are able to use an inductive sensor to measure electrical impedance and relate it to the electrical properties of printed ink structures. By combining the electrical measuring system with another (such as optical) into a single metrology system for evaluating film properties, with extra thickness and lift-off data, it would be possible to extract the actual electrical resistivity of printed tracks and films.

A range of samples with varying values of resistivity and height were fabricated by screen printing. Using a surface profiler the height of our samples were measured, typical examples can be seen in Table 1; additionally the resistance between two fixed-position probes was measured on a probe station. In the example shown here, sample 5 contains no silver whereas the remaining samples contain varying amounts of silver and carbon such that a range of values of resistivity could be investigated.

The inductive sensor was based on a 100 µH inductor (7.5 mm diameter) which had its cap removed to expose the coil. Using an impedance analyser the frequency response of the inductor between 8.5 to 11 MHz (this range covers the resonant frequency of the inductor) was monitored with an air gap between the sensor and sample of ~20 µm. The maximum impedance measured within this frequency range is plotted in Figure 1 against the sheet resistivity.

The red line in Figure 1 shows the value of the impedance the bare substrate. This data clearly shows that values of sheet resistivity below 8 Ω/square can be detected using this technique.

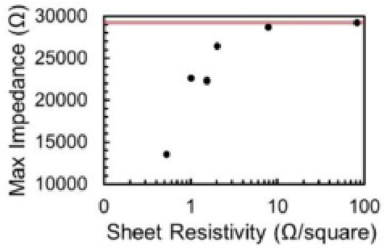
Contactless inductive sensing using eddy currents can provide information on changes in the electrical properties of samples. This makes it feasible to measure the electrical properties which at present are not monitored in roll-to-roll printed electronics manufacture.

[1] D. Savastano, "*Conductive Inks Drive Growth in Flexible and Printed Electronics*", Printed Electronics Now, March 2015

Table 1: Height and sheet resistivity values of samples measured before test

Sample	Height (µm)	Sheet Resistivity (Ω/square)
1	18	1.6
2	12	0.5
3	21	7.8
4	15	2.0
5	11	82.1
6	8	1.0

Figure 1: Graph showing measured impedance v sample sheet resistivity



(P.15) Flexible Large Area OLED and OPV Devices Manufactured by Thermal Evaporation and Spin-coating, using Flexible ITO-free TCO Electrode

Paolo Melgari[1], (Sam) Yun Fu Chan[1], Phil Hollis[1], Parnia Navabpour[2], Kevin Cooke[2], Joanne Stallard[2], Sue Field[2], Alexander Goruppa[3], Katrin Zorn[3], Manuel Auer[4], Andreas Klug[4], Emil J.W. List- Kratochvil[4,5], Guosheng Shao[6]

[1]Centre for Process Innovation (CPI), Sedgefield, United Kingdom, [2]Teer Coatings Ltd, Miba Coating Group, Droitwich, United Kingdom, [3]High Tech Coatings, Miba Coating Group, Vorchdorf, Austria, [4]NanoTecCenter Weiz Forschungsgesellschaft mbH, Austria, [5]Institute of Solid State Physics, Graz University of Technology, Austria, [6]University of Bolton, Bolton, United Kingdom

Keywords

ITO-free, OLED, OPV, Large area, Barrier, HTL

Abstract

A multi-layer film of ITO-free TCO was deposited onto polyethylene naphthalate (PEN) substrate by Physical Vapour Deposition (PVD) using Closed Field UnBalanced Magnetron Sputtering (CFUBMS) obtaining coatings with resistivity in the order of 10^{-4} Ω·cm, and with transmission in the visible spectrum greater than 85%. Alumina- and hybrid silica-based barrier films were deposited by PVD and PACVD (Plasma Assisted Chemical Vapour Deposition).

These substrates were used for manufacturing flexible large area OLED (Organic Light Emitting Diode) and OPV (Organic Photovoltaic) devices based on a novel semiconducting Hole Transporting Layer (HTL) and other films coated by a combination of thermal evaporation and spin-coating on CPI's OLED/OPV prototyping line. Individual device dimensions were up to 8 inches.

Biography

In my current position at CPI, I'm employed as Process Scientist developing large area optoelectronic devices manufactured and encapsulated by a range of techniques including Atomic Layer Deposition.

My background is in Chemistry (specifically synthesis of organometallic compounds) and development of Chemical Vapour Deposition (CVD) technologies for rigid and flexible substrates. I gained MSc in Chemistry at University of Parma (Italy), I took part in ERASMUS exchange program at University College of London (UCL) and subsequently decided to start PhD in Chemistry on developing CVD in the same University (Thesis not submitted yet).

I worked for over 4 years in the photovoltaic industry developing coating technologies for solar cells from small scale (1"-square) up to full industrial scale.

(P.16) Effect of grain boundary position on the drain current of polysilicon source-gated transistors

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Source-gated transistors (SGTs) [1-3] have extensive benefits to both digital and analog applications due to their current control mechanism. This includes tolerance to processing variability and bias stress.

Here we show that the drain current of SGTs made in polycrystalline silicon has comparatively small sensitivity to the position of a crystalline grain boundary. This should result in improved uniformity of SGT performance compared to conventional polysilicon TFTs [4-5].

Silvaco Atlas was used to create a 2-d representation of a polysilicon SGT comprising a Schottky potential barrier at the source. To simulate the grain boundary, a short (20nm) defective region was created in the semiconductor (crystalline silicon) and its position was swept across the *x*-axis of the device, as shown in Fig. 1.

We computed electrical characteristics for the transistors for every position of the grain boundary, stepping 10nm in the *x* direction. Figures 2 and 3 show the results of these sweeps.

The lowest current is obtained when the grain boundary is close to the right-most edge of the source. This is known to be the most important area of the device. However, the maximum drop in current for this structure was approx. 14% and this occurs for very specific positions of the grain boundary close to the edge of the source (a comparatively small portion of the device in the *x* direction).

Statistically, we expect SGT devices to perform robustly, with low device-to-device variation due to randomness of grain boundary position when realized in polycrystalline materials.

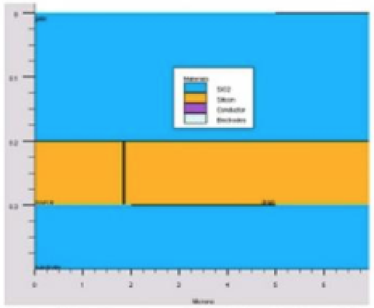

Fig. 1. Schematic cross-section of the simulated SGT, showing the position of the movable defective region.

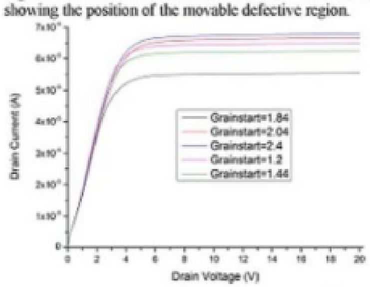

Fig.2. Output characteristic for V_G = 5V and different positions of the grain boundary. x = 2μm represents the edge of the source closest to the drain.

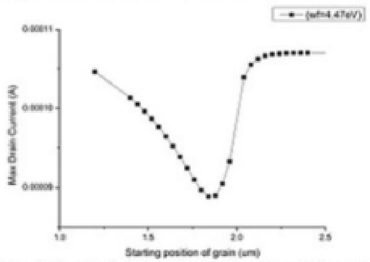

Fig. 3. Saturated drain current vs position of the grain boundary for V_G = 5V.

Acknowledgements

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References

1. J. M. Shannon and E. G. Gerstner, *IEEE Electron Device Letters* 24, 405–407, (2003).
2. R. A. Sporea et al., *Sci. Rep.* **4** 4295 (2014).
3. R. A. Sporea et al., *Sci. Rep.* **5** 14058 (2015).
4. P. C. van der Wilt, B. D. van Dijk, G. J. Bertens, R. Ishihara, *Applied Physics Letters* 79, 1819, (2001).
5. G. A. Armstrong et al., *IEEE Electron Dev. Lett.*, 18, 315–318, (1997).

About the Authors

This work was done during a summer research placement by Luke Wheeler who at the time was 17.

Luke Wheeler was a sixth form student at Woking College.

Dr Radu Sporea is Royal Academy of Engineering Academic Research Fellow at the Advanced Technology Institute (ATI). Current interests include printed and flexible large-area electronics, contact effects, modelling and simulation, and energy-efficient analog circuits. Radu received the Isambard Kingdom Brunel Award and Lecture for Engineering from the British Science Association in 2015 and the EPSRC RISE Rising Star distinction in 2014.

(P.17) OPCAP: Offset lithographic printing of high-k dielectric capacitors

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iSMART: Innovations in Surfaces, Materials and related technologies
Nottingham Trent University

Abstract
Printed hybrid flexible electronics combine conventional silicon based microelectronics and sensors with printed conductive electrodes, sensors and passive electronic components on low cost plastic substrates. Intelligent labels providing combinations of anti-counterfeit measures, track and trace features, tax stamp authentication and supply chain control and authentication would benefit from printed passive electrical components, rather than pick and place of discrete devices. Resistors and inductors can be printed by careful patterning with conductive and insulating inks, but printed capacitors are more challenging. The research investigates the feasibility of producing a UV cured ink for industrial offset lithographic printing presses and optimising in-line photonic sintering techniques to create parallel plate printed capacitors on plastic sheets.

(P.18) Spray coated silver nanowires as transparent electrodes for printed PVs on opaque substrates

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Keywords: Transparent conducting films, transparent electrodes, silver nanowires, spray coating, Organic photovoltaics

Abstract: Most transparent conducting electrodes (TCEs) currently use ITO based electrodes, which have limited conductivity and possess too high a cost for widespread commercialisation in many applications. Furthermore, ITO has limited longevity on polymer substrates and can be a limiting factor in the lifetime and subsequent value of a product. Therefore, a number of alternatives have been researched and amongst them, silver nanowires (AgNWs) has emerged as a viable alternative to ITO due to the low cost, reliability and low sheet resistance.

In this presentation, the use of silver nanowires (AgNWs) as an alternative to ITO for applications in Organic Light Emitting Diodes (OLEDs), Organic Photovoltaics (OPVs) and Perovskite Solar Cells (PSCs) is discussed. Dispersions of the AgNWs have been used to prepare thin, flexible, transparent and conducting films using spray coating. Control of the spray parameters allows a low sheet resistance to be obtained onto a PET substrate (R_S = 15 Ω/sq.), whilst maintaining high optical film transparency (T = 89% @ λ = 550nm). Owing to the light-scattering influence of the AgNWs, the density of the AgNW network can also be varied to enable controllability of the optical haze through the sample. Based on the identification of the optimal haze value, OPVs and PSCs have been fabricated using the AgNWs as the transparent electrode and have been benchmarked against ITO electrodes.

A further advantage of the spray coating process is that the material can be directly deposited onto active layers by selecting a solvent that possesses orthogonality with the underlying organic layer. This is particularly important for applications where a semi-transparent final device is required, or an opaque substrate is used. Two such examples will be presented in this presentation; firstly, semi-transparent devices, where both the front and the rear electrodes are transparent and secondly, a PSC, which is fabricated directly onto a low-cost steel substrate. In both cases, the efficiency of the devices is comparable to that made on a glass sample with an ITO electrode.

(P.19) Solution-Processed Co-planar Nano-Scale LEDs by Adhesion Lithography (a-Lith)

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As the resolution of devices in the electronics industry has hit the nanoscale, device fabrication costs have rapidly increased. Whilst commercial technologies such as photolithography are able to produce nanoscale feature size, they are costly and unsuitable for large area printable electronics. Concurrently in the display and lighting industries there is a strong focus on developing high throughput low cost optoelectronic devices for next generation technologies.

Adhesion Lithography (a-Lith) is a simple fabrication technique that uses unique properties of self-assembled monolayers (SAMs) to create planar electrodes separated by sub 10nm gaps[1]. Using this novel electrode fabrication technique in conjunction with solution processable semiconductors, highly scalable, low-cost, lateral architecture organic light-emitting diodes (OLEDs) are demonstrated. Green, red and blue a-Lith nano-LEDs were fabricated via spin coating of various state-of-the-art electroluminescent polymers, including: poly[(9,9-di-n-octylfluorenyl-2,7-diyl)-alt-(benzo[2,1,3]thiadiazol-4,8-diyl)] (F8BT), poly[2-methoxy-5-(3',7'-dimethyloctyloxy)-1,4-phenylenevinylene] (MDMO-PPV) and poly(9,9-di-n-octylfluorenyl-2,7-diyl) (PFO), respectively . Several hole and electron transport/blocking layers were implemented to improve the efficiency of the nano-LEDs.

The combination of a-Lith with these materials, demonstrates the capability of this simple highly reproducible technique to create nano-junction LEDs and shows great promise for large scale printable high density LEDs for ultra-high resolution display technology and sensor applications.

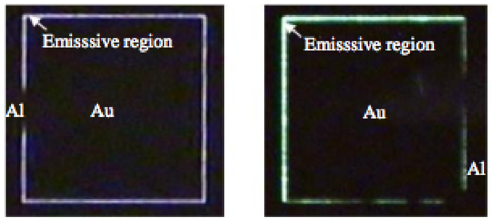

Fig. 1: *PFO- and F8T2-based nano-OLEDs*

1. D. J. Beesley et al. "Sub-15-nm patterning of asymmetric metal electrodes and devices by adhesion lithography.," *Nat. Commun.*, vol. 5, p. 3933, Jan. 2014.

Biography

Gwenhivir Wyatt-Moon is studying a PhD in Physics as part of the Advanced Materials and Devices group at Imperial College London. She received a BEng in Electrical and Electronic Engineering from Swansea University. Subsequently she worked for a medical start-up company developing novel gas sensors and rheometry equipment. She then went on to complete an MRes in Plastic Electronics at Imperial College London. Her current research interests include novel fabrication techniques, materials and devices for the plastic electronics field.

(P.20) Laser Direct Writing of RF Passive Components on Flexible Substrates

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Keywords: Laser Sintering, Laser Ablation, Co-Planar Waveguides, RF passive components

Abstract
Flexible electronics have emerged as a very promising alternative of CMOS compatible electronics for a plethora of applications. Laser microfabrication techniques, such as Selective Laser patterning and Sintering are compatible with flexible substrates and have demonstrated impressive results in the field of flexible electronic circuits and sensors. However, laser based manufacturing of RF passive components or devices is still at an early stage. At the same time, despite the impressive advancement of RF systems over the past decade, there are still substrate -related issues which are impeding their further performance increase In this work we report on the all-laser fabrication of Silver Co-planar Waveguides (CPWs) on Poly-EthyleneNapthalate (PEN) substrates employing flat-top optics to achieve uniform laser fluence and thus high fabrication precision and reproducibility but also to mitigate the thermal effects of nanosecond laser pulses. The CPWs have been fabricated to match the impedance of 50Ω ports of an Anritsu Vector Network Analyzer operating from 40MHz - 40GHz. The all laser fabrication process consisted in the selective laser sintering of square dies on a Silver Nano Particle layer spin-coated on a PEN substrate followed by the selective laser patterning of the CPWs with a ns pulsed Nd:YAG laser source operating at 532nm, according to the optimized parameters extracted from a previous studies of the authors (Figure 1). The CPWs have been characterized electrically at the 0.04-40GHz regime and found to be excellent transmission lines with a 40GHz 3dB bandwidth, owing to the high electrical conductivity of Ag and the excellent dielectric properties of PEN. This novel process is a milestone towards the RF technology transfer to flexible electronics with low cost and specs comparable or even superior to the CMOS compatible equivalents. The proposed structures are of interest for WLAN bands, between 2.4 and 5.9 GHz, but also for high frequency (>25 GHz) applications.

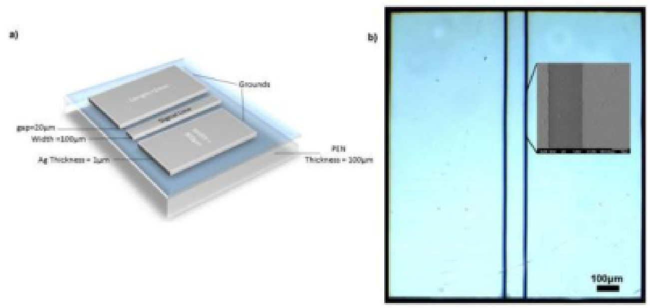

Figure 1. a) CPW specs and b) actual microscope photograph on PEN substrate; the patterns' line edge roughness is in the order of 1µm.

Biography

Dr. Filimon Zacharatos (male) is currently a post-doctoral researcher at the Physics Department of NTUA in the frame of the European Marie Curie project "LaserMicroFab". He received the Physics diploma from Patras University in 2003 and his Ph.D. degree, specializing in nanotechnology for microelectronics and RF systems, from the Applied Physics department of the National Technical University of Athens (NTUA) in 2009. Between 2011 and 2013 he worked as a postdoctoral fellow in the sub-micron optics group of ICB/CNRS at the University of Burgundy, working on hybrid plasmonic-photonic systems. His current research is focused on the Laser Direct Writing of electronic devices and sensors on flexible substrates using metal nanoparticle inks. He is the author or the co-author of 12 publications in peer-reviewed journals, of 6 publications in conference proceedings, 1 book chapter and he is the co-inventor of 1 patent.

(P.21) Development of a Method for the Manufacture of Hybrid Energy Storage Using 3D Printing Technology

Milad Areir*, Yanmeng Xu*, Eujin Pei, David Harrison, John Fyson, Anan Tanwilaisiri and Ruirong Zhang

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Abstract
This research intends to develop a method for the manufacture of a hybrid energy storage and heating device that can be used for preventing the accumulation of ice and snow in residential areas, e.g. rooftop or playground. The major contribution of this work will be the development of an effective method of preparing complex hybrid structures for smart energy storage using 3D printing technology, and to develop composite materials for the hybrid structure and energy storage. 3D printing allows free form fabrication of complex hybrid structures which will be used to produce "smart bricks" or a "smart mat". The 3D printing processes, including the printing speed and the distance between nozzle and substrate, will be investigated to control the layer uniformity and complex structure of the energy storage device. The electrical and thermal properties of the device will be measured to evaluate its efficiency at providing heat. Carbon material will be used as the energy storage material electrodes and different types of the carbon materials will be investigated in order to optimise the energy storage capacity.

Keywords:
Hybrid Energy Storage, 3D Printing Technology, Smart Bricks, Energy Storage Material

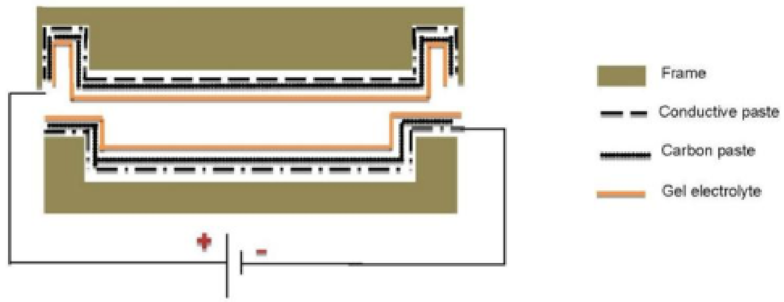

Figure Schematic diagram of 3D printed energy storage.

Biography

Milad M. Areir is a PhD student in College of Engineering at Brunel University London. He received a Master's degree in Electrical Engineering from the University of Engineering and Technology Taxila, Pakistan. Prior to beginning the PhD program, he worked as an instrument engineer at Reda Fire and Safety, as well as a part-time Lecturer at Msalata Technical Institute-Libya. Milad is currently interested in the research area of printing materials and devices using the 3D Printing Technology.

(P.22) Energy Harvesting with Plastic Electronics

Stuart Higgins; Henning Sirringhaus

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In this presentation I will review the current state-of-the-art both in organic and inorganic rectifiers, as well as discuss recent results from our group on printed high-speed rectifying diodes, based on a high-mobility polymer.

Plastic electronics have long been hailed as the solution to the relatively high manufacturing cost of radio tags. The argument is that additive manufacturing of rectifying circuitry directly onto substrate can undercut the current limiting cost of attaching discrete silicon chips to antennas. Hence plastic electronics has an 'unfair advantage' over the markets of radio frequency identification (RFID) tags and energy harvesting.

However nearly ten years after this initial argument, the widespread adoption of plastic electronics in RFID hasn't occurred. In terms of organic semiconductors the fundamental challenge is fabricating rectifiers, either from diodes or transistors, which switch fast enough to capture the energy emitted by high frequency radio waves. Chief among the factors affecting speed is a familiar problem: the poor mobilities of organic semiconductors, hindered further by the disparity between field-effect and vertical charge transport. Similarly other less-oft considered factors such as device architecture, particularly in the case of transistors, significantly influence switching behaviour.

I will discuss different approaches to overcoming these issues, both through different device architectures, materials, and fabrication methods including inkjet printing.

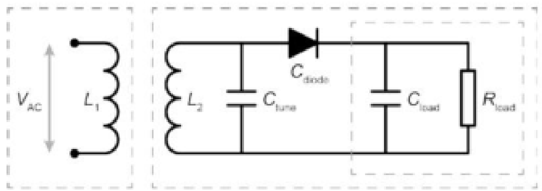

Figure:
Simplified schematic of an energy harvesting/rectifying tag, showing the key components

Keywords:
energy harvesting, organic diode, high-frequency, rectification, RFID

Biography

Stuart Higgins is a Research Associate at the University of Cambridge, within the group of Professor Henning Sirringhaus. Stuart specialises in the fabrication and characterisation of organic devices on plastic, currently focusing on organic diodes for use in energy harvesting. He completed his PhD in 2014 in the Department of Physics at Imperial College London under the supervision of Dr Alasdair Campbell, where he developed megahertz switching organic field-effect transistors on plastic, using a combination of nanoimprint lithography, self-aligned processing and gravure printing. Outside of academia Stuart is a keen broadcaster, producing audio interviews with academics.

(P.23) Flexipower: Printed Radio Frequency Energy Harvesting

Tim Mortensen, Philip Cooper

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Abstract

The development of energy harvesting systems has been of increasing importance in recent years, and with the push towards the internet of things (IoT) and the development of ultra-low cost printed electronics the number of potential applications for such systems is rapidly growing.

The FLEXIPOWER project aims to produce a fully printed radio frequency (RF) energy harvesting system for use with printed electronic devices and as an alternative to conventional batteries in traditional electronic devices. The system requires an antenna tuned to the desired RF frequency, typically 13.56MHz, 433MHz, 900MHz or higher, a compatible rectifying circuit, smoothing circuitry and an energy storage device.

Due to the high frequencies involved and limited available voltage a high speed Schottky diode is desirable. These diodes are typically used in high frequency applications and have the additional benefit of a low forward voltage drop. However, these specifications have long been challenging to produce using printing techniques.

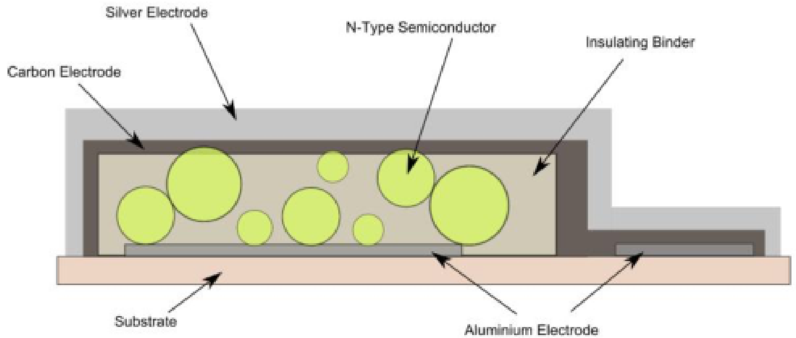

Figure 1 - Schematic of a printable Schottky Diode

We describe the design and progress towards a fully printed radio frequency energy harvesting system, with a focus on recent work creating high frequency diode. The featured diode is created using techniques and materials with the potential to scale to production via large area electronics manufacturing techniques, including screen printing and patterned vapour deposition. Such a component would be the first step in towards the FLEXIPOWER goal of producing a small and flexible, entirely printed, energy harvesting system for use in ultra-low cost applications where traditional electronics are currently prohibitively bulky, expensive and damaging to the environment.

(P.24) Polymer-Sorted Semiconducting Single Walled Carbon Nanotubes for Next-Generation Flexible Nanoelectronics

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[3]Institute of Physical and Theoretical Chemistry, Julius-Maximilian University Würzburg, Würzburg, Germany

Abstract
Single walled carbon nanotubes (SWNTs) have attracted a lot of attention in the last years, owing to their unique mechanical, thermal and opto-electronic properties. The ability to disperse SWNTs in water and in organic solvents makes solution-based processes very promising for the fabrication of SWNT-based devices. Here, we demonstrate the technological potential of solution-processed semiconducting SWNTs with single chirality sorted and dispersed by means of conjugated polymer wrapping[1].

By employing a solution deposited network of polymer-sorted SWNTs, we fabricate and characterize transistors and integrated circuits (**Fig. 1**) on rigid as well as free-standing flexible plastic substrates, bent down to 4 mm[2]. Complementary-like logic circuits[3] have also been realized by integrating, on the same flexible substrates, polymer-sorted SWNTs with various semiconducting oxides, like IGZO and InO_x (**Fig. 2a,b**). Moreover, optoelectronic devices, such as blue color light-emitting diodes, have also been realized combining these polymer-sorted SWNTs with a novel nano-gap device architecture realized by adhesion lithography[4], a novel and highly scalable patterning technique (**Fig. 2c**).

Our work highlights the tremendous potential of polymer-sorted SWNTs for applications in plastic and flexible nanoelectronics.

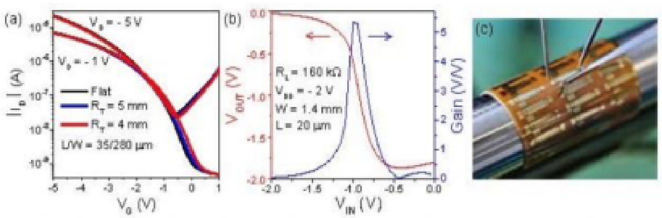

Figure 1: (a) Transfer characteristic of a flexible SWNT transistor, measured while flat and bent to tensile radius down to 4 mm. (b) Voltage transfer characteristic and corresponding static gain of a SWNT unipolar voltage inverter. (c) Photograph of the actual flexible devices during testing.

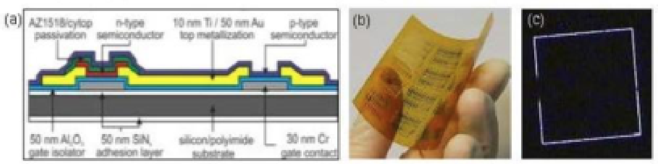

Figure 2: (a) Schematic cross-section of a hybrid complementary inverter based on solution-processed p-type SWNT and n-type metal-oxide. (b) Photograph of the entire processed free-standing mechanically flexible foil. (c) Photograph of light-emitting nano-gap diode supplied at -14V.

[1] A. Nish, *et al.*, Nature Nanotechnology **2**, p.640, (2007). [2] F. Bottacchi, *et al.*, Applied Physics Letters **106**, 1933027, (2015). [3] L. Petti, *et al.*, IEDM, p.26.4.1, (2014). [4] D.J. Beesley, *et al.*, Nature Communications **5**, p.3933, (2014).

Biography

Francesca Bottacchi is a PhD student in Experimental Solid State Physics at Imperial College London with a Marie Curie fellowship, under the supervision of Professor Thomas Anthopoulos. She received her BSc and MSc with honours in Physics Engineering - Nanotechnology and Physical Technologies from Politecnico di Milano (Italy) in 2011 and 2013, respectively. During her master thesis at Istituto Italiano di Tecnologia - Centre for Nano Science and Technology in Milan (Italy), she worked on single walled carbon nanotubes based hybrid solar cells, under the supervision of Professor Guglielmo Lanzani. She is currently working on single walled carbon nanotube - conjugated polymer functional systems for nano-scale electronics and photovoltaics, as part of a European project called POCAONTAS (Polymer-Carbon Nanotube Active Systems for Photovoltaic).

(P.25) Stretchable, transparent and conductive graphene film

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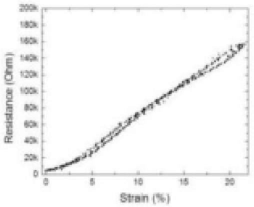
Abstract

Stretchable electronics is a rapidly expanding research area[1]. Stretchable and transparent conductive electrodes (TCEs) are extremely needed in applications such as electronic skin, sensors, actuators, photovoltaic cells, light emitting diodes, and electronic textiles.[2] However, the inherent limitations in the electrical and mechanical properties (electrical conductivity under strain lower than tens of S/m and fracture strain lower than 5%) of conventional TCEs (e.g. Indium-Tin Oxide, Aluminum Oxide, etc.) make them unsuitable for stretchable applications and motivates the efforts to look for alternative transparent conductive materials.[2] The electrical, optical and mechanical properties of graphene are ideal for transparent, stretchable conductive electrodes[3,4]. Here we present a novel graphene-based stretchable transparent conductor bonded on a substrate of polydimethylsiloxane (PDMS). A Graphene ink is produced by liquid phase exfoliation of graphite in water/surfactant solution[5,6]. Transmission electron microscopy and Raman spectroscopy reveals that the ink is composed of ~33% single layer graphene flakes. The conducting graphene film is prepared by filtering the graphene ink through a filter membrane. The dried membrane carrying the graphene film is then transferred onto a PDMS film (100μm thick) and the filter is dissolved. We found that the graphene film adheres to the PDMS due to hydrophilic interactions. The optical transmittance of the graphene-PDMS stretchable conductor is about 70% in the visible range. The PDMS bonded graphene films remain conductive when subjected to tensile strains of at least 25% (Sheet $resistance_{25\%}$=19xSheet $resistance_{0\%}$). The graphene films also survive more than 1000 multiple strain cycles of to 25% uniaxial strain without significant changes in the strain versus resistance behavior. These stretchable and transparent graphene on PDMS conductors are promising for applications as contact electrodes for a novel class of intrinsically stretchable electronic components such as compliant organic LEDs. They may also be integrated as interconnects or strain sensors in elastic electronic skins.



(a) (b)

Fig.1: a) Graphene-ink, b) Graphene stretchable TCE under electro-mechanical test, c) Resistance vs strain curve for graphene stretchable TCE

References

[1] T. Someya, *Stretchable Electronics*, First Ed., Wiley-VCH Verlag, 2013 [2] D.H. Kim *et al*, Adv. Mater., 20 (2008).
[3] F. Bonaccorso *et al*. Nat. Photon. 4 (2010) 611.
[4] K. S. Kim *et al*. Nature 457 (2009), 706.
[5] J.N. Coleman *et al*. Nat. Nanotechnol. 3 (2008) 563. [6] F. Torrisi *et al*. ACS Nano 6 (2012) 2992

Biography

Tian Carey is a research student working towards a PhD in the EPSRC Centre for Doctoral Training in Graphene Technology. He is in the Cambridge Graphene Centre in the Electrical Engineering Division and a member of Pembroke College. He graduated with a MPhil degree in micro and nanotechnology enterprise from the University of Cambridge, Department of Materials Science, after studying in Ireland at University College Dublin.

(P.26) Solution-processed, centimeter-sized, single-crystalline layers for high-performance organic thin-film transistors

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Driven by the high potential of single-crystalline organic semiconductors for efficient charge transport in high performance devices, several techniques have recently been developed to deposit single-crystalline thin films of organic semiconductors on large area. Among them, meniscus guided coating techniques have shown the possibility to grow inch-sized highly-crystalline organic thin films.[1] There, a droplet of semiconductor solution is dragged across the substrate. The crystal formation occurs along the receding meniscus front.

In this work, we use a homebuilt zone-casting setup to grow films of the commercially available organic semiconductor C_8-BTBT. This setup employs a slot-die coater, which can be used to resupply the semiconductor solution in order to keep the droplet shape constant. This permits the fabrication of highly crystalline layers on arbitrary substrate sizes, enabling large area fabrication. Optimization of this process leads to C_8-BTBT films with crystalline domains in the range of several millimeters. OTFTs fabricated on these layers showed well behaved transistor characteristics with maximum charge mobilities reaching 7 $cm^2V^{-1}s^{-1}$ and with good film uniformity as 75 transistors distributed across a single sample show an average mobility of 4.4 $cm^2V^{-1}s^{-1}$.

To further optimize the crystallinity, we employed a similar technique as recently shown by Diao and coworkers.[2] We selectively pattern arrays of solvent-wetting regions next to non-wetting areas. This allows better nucleation control resulting in higher crystallinity. Remarkably there is no further fluid-flow enhancement required in our technique, as coating speeds are in the range of 100 µm/s.

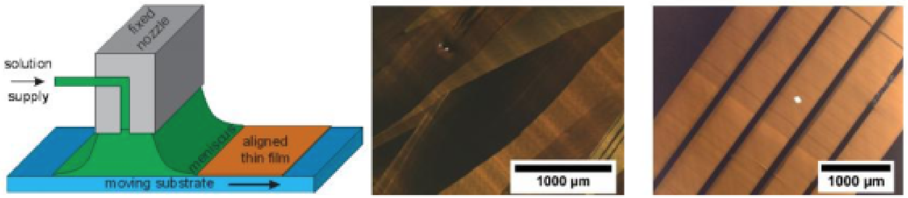

Figure 1: (a) Illustration of the zone casting setup. (b, c) Cross-polarized light microscopy images of the C_8-BTBT single crystal without (b) and with (c) substrate patterning. The white arrow indicates the coating direction.

References

1. Soeda, J. *et al.*, *Appl. Phys. Express* **6,** 2-ɔ (2013).
2. Diao, Y. *et al.*, *Nat. Mater.* **12,** 665–71 (2013).

Biography

Robby Janneck started studying physics at TU Dresden in 2008. During his studies he held various research assistant positions in the field of organic electronics at TU Dresden, University of Florida, Novaled and Fraunhofer. After finishing his master studies in 2014, he joined IMEC as a PhD researcher in the large area electronics department under supervision of Paul Heremans and Jan Genoe. He is now working in the framework of the "Epos Crystalli" ERC project on high performance, single-crystalline organic thin-film transistors.

(P.27) High Mobility Solution-Processed Organic Small Molecule-Polymer Blend Thin-Film Transistors with Hole Mobilities of up to 13 cm^2/Vs

Alexandra F. Paterson, Weimin Zhang, Martin Heeney, Iain McCulloch, Neil D. Treat, Olga Solomeshch, Nir Tessler, Thomas D. Anthopoulos

Department of Physics and Centre for Plastic Electronics, Blackett Laboratory, Imperial College London, London SW7 2BW, United Kingdom

Abstract

Plastic electronics that can be manufactured using solution-based methods are the subject of great research interest due to their potential for low-cost, large-area electronic applications. The interest in this field has led to considerable research and subsequent advances in device performance. To this end solution-processed organic thin-film transistors (OTFTs) have shown impressive improvements in recent years through the increasing values of charge carrier mobility. Here we report the development of next generation organic blend materials for spin-coated OTFTs with hole mobilities of up to 13 cm^2/Vs. These high performance devices have been achieved using a novel tertiary semiconducting blend system comprising of an amorphous-like conjugated polymer, a highly crystalline small molecule and a fluorinated fullerene as a dopant. The combination of a highly crystalline small molecule with the polymer binder aids the formation of uniform films as well as enables an element of control over the nucleation and growth of the small molecule; a solvent-blending approach is also employed to further control the nucleation and growth processes, having a significant effect on the morphology of the blend and subsequent mobility of the OTFTs. The polymer binder that has been used is indacenodithiophene-benzothiadiazole (C_{16}IDT-BT), which belongs to the family of indacenodithiophene-based copolymers which are renowned for their high carrier mobilities regardless of their apparent structural disorder. 2,7-Dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C_8-BTBT) has been carefully selected as a complementary small-molecule to blend with the C_{16}IDT-BT and furthermore, the inclusion of $C_{60}F_{48}$ as a molecular dopant within this system has greatly improved device characteristics. These organic devices provide an interesting insight into this complex blend system, highlighting the correlation between the morphology developed following solution processing and device performance, as well as demonstrating the potential of this novel tertiary blend system.

Biography

Alexandra F. Paterson is a third year PhD student at Imperial College London under the supervision of Professor Thomas Anthopoulos. Alexandra's work focusses on high-mobility organic thin-film transistors using blends consisting of a small-molecule and a polymer.

Keywords

morphology, organic thin-film transistor, small molecule polymer blend, high mobility, dopant

Acknowledgements
The authors are grateful to Cambridge Display Technology Ltd (Company Number 2672530) for the financial support.

(P.28) Transfer Printing Si Nanowires for Flexible Large Area Electronics

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Abstract

Si nanowires (NWs) are promising building blocks for high-performance flexible electronics due to single crystallinity, low dimensionality, high surface-to-volume ratio, as well as, excellent electronic properties and compatibility with CMOS fabrication technology. Variety of top-down and bottom-up synthesis methods have been developed for the synthesis of Si NWs. Since the direct synthesis of high crystal quality NWs on flexible substrates is hindered by thermal budget requirements, a range of approaches have been explored for transferring aligned NWs from planar (growth substrate) to flexible substrates[1]. The high-performance functional circuits require assembly of highly aligned NWs along the surface of the substrate and high density at defined locations on the substrate[2].

In this work, we present the assembly efficiency of Si NWs, synthesized by top-down metal-assisted chemical etching (MACEtch) method (Fig.1) and on transfer printed on flexible substrates. The tape peeling (Fig. 2) and the contact printing (Fig.2) techniques were used to obtain printed arrays of aligned NWs on flexible substrates. We studied the scalability of both techniques to explore the printing of NWs based flexible electronics on large areas.

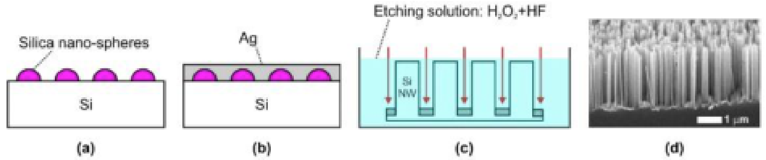

Fig. 1. (a-c) Schematic of MACEtch process, and (d) SEM image of Si NWs.

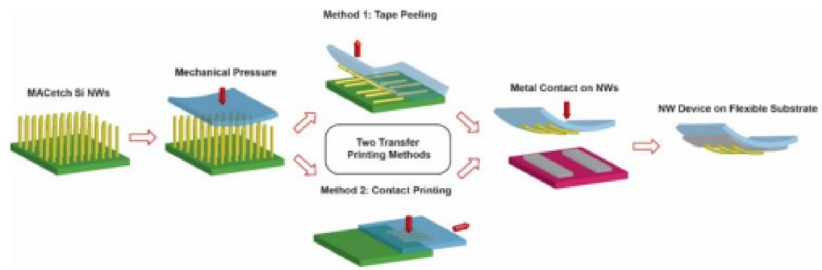

Fig. 2. Schematic of the tape peeling (method 1) and contact printing (method 2) techniques.

References
[1]R. S. Dahiya *et al.*, Microelectronic Engineering, vol. 98, pp. 502-507, 2012.
[2]Ali Javey, *et al.*, Advanced Materials, vol. 21, pp. 3730-3743, 2009.

Keywords
Si nanowires (NWs), Si etching process, Top-down NW synthesis, NW transfer printing,

Biography

Dr. Dhayalan Shathivel, studied M.Sc Materials Science at Bharathiyar University, Coimbatore, India. He received his Ph.D in 2014 from the Indian Institute of Science, Bangalore, India, working on growth of semiconducting nanowires by vapour-liquid-solid (VLS) mechanism using CVD method. His main research work focused on physical chemistry aspects of vapour-liquid-solid growth of nanowires which received good attention. Currently, he is working as a postdoctoral researcher at the School of Engineering, University of Glasgow, United Kingdom. His current research interests includes transfer printing of semiconducting nanowires for flexible electronics applications.

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(P.29) Copper(I) thiocyanate (CuSCN) as a hole-transport layer material for large- area opto/electronics

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Abstract
Recent advances in large-area opto/electronics have demonstrated the potential of copper(I) thiocyanate (CuSCN) as a universal hole-transport layer (HTL) material for applications including transparent thin-film transistors (TFTs) and perovskite-based photovoltaic cells [1]. CuSCN is an inexpensive inorganic, p-type semiconductor that exhibits good hole-transport properties. This molecular material has a large bandgap (>3.5 eV) that facilitates high optical transparency across the visible to near infrared region of the electromagnetic spectrum [2]. Its wide availability combined with its processing versatility makes CuSCN ideal for large-area opto/electronic applications.

CuSCN has a unique combination of attractive characteristics, but reports on organic photovoltaic (OPV) cells utilising CuSCN are extremely limited. Recent advances in OPV research have resulted in power conversion efficiencies (PCE) exceeding 10%, and most high efficiency OPVs use poly(3,4-ethylenedioxythiophene): polystyrenesulfonate (PEDOT:PSS) as the HTL. However, the stability of these cells can be limited by PEDOT:PSS reacting with the anode electrode [3] or the active layer [4]. Consequently, further progress in this field requires the development of alternative HTL materials that can increase both device lifetime and PCE.

Here we report on the use of CuSCN as an HTL material in solution-processed TFTs and high efficiency OPV cells. We were able to modify the conductivity and work function of CuSCN films with the addition of suitable chemical dopants; hole mobilities exceeding twice that of pure CuSCN were demonstrated in TFTs with optimised doped systems. The identification of inexpensive solvents that facilitate the production of high concentration CuSCN solutions (10–40 mg mL^{-1}) enabled the deposition of HTL with controlled thickness. We were able to use these novel formulations to solution-deposit pure and doped CuSCN films with high uniformity over large-area substrates at 100 °C. Field-effect TFT measurements allowed us to assess the charge transport properties of CuSCN films. Combining TFT measurements with other thin-film analysis techniques enabled us to optimise fabrication parameters and improve the performance of our devices. Average optical transparencies approaching 90% (400–1300 nm) were measured for CuSCN-based HTL interlayers; this is significantly higher than the value measured for standard PEDOT:PSS interlayers. Bulk heterojunction OPV cells with optimised CuSCN-based HTL demonstrated PCE in the range 6-8%, which are superior to PCE measured in reference OPV cells with PEDOT:PSS HTLs. The dramatically enhanced OPV performance we observed was attributed to the excellent transparency and electron blocking properties of CuSCN. Hence, this work demonstrates the tremendous potential of CuSCN as an HTL material for next generation large-area opto/electronics.

[1] N. Wijeyasinghe & T.D. Anthopoulos, Semicond. Sci. Technol., **30**, 104002, 2015. [2] P. Pattanasattayavong, et al., Adv. Mater., **25**, 1504, 2013.
[3] M.P. de Jong, et al., Appl. Phys. Lett., **77**, 2255, 2000. [4] A. Garcia, et al., Adv. Mater., **24**, 5368, 2012.

(P.30) High resolution high velocity laser printing of metal lines

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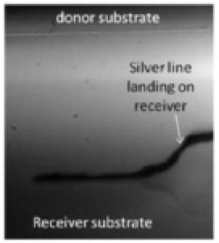
Keywords: laser printing; interconnection; fast imaging; silver inks

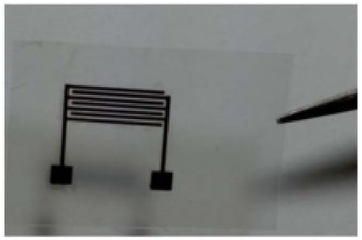
Abstract

The deposition of conductive lines of few tens of micrometers width is of prime interest for the manufacturing of electronic devices, especially on flexible substrates. Laser printing, based on LIFT process (Laser-Induced Forward Transfer), appears very attractive for such application. This technique allows the deposition of silver nanoparticle inks with a wide range of viscosities [1] and the formation of 2D/3D structures with high resolution [2].

Recently, micrometer conductive lines have been laser printed at velocities up to 4 m/s in multi-passes configuration with a picosecond laser operating at 500 kHz and a scanning mirror to move the laser at the surface of the donor film [3]. Time-resolved shadowgraphy [4] is the best technique to investigate the dynamics of formation and expansion of the liquid jet. Such studies showed that the instabilities induced by the interactions between two adjacent cavitation bubbles and/or two adjacent liquid jets prevent the deposition of a continuous line in a single step at high velocity with standard silver nanoparticle inks (20% silver content) [5, 6]. In this study, we investigate the influence of silver ink donor film properties (thickness, metal content) on the dynamics of the liquid transfer at high velocity and the morphologies of the printed lines. In particular, we observe a new deposition mechanism when we use inks with higher densities (40% silver content) to print conductive lines at high velocity. When a laser pulse impacts the edge of the bubble generated by a previous pulse, it increases the cavitation bubble volume and forms a continuous line flying from the donor to the receiver substrate (fig. 1). In these conditions, we printed 30 µm width silver lines at velocities up to 17 m/s in a single pass, using a UV picosecond laser operating at 1 MHz (fig. 2).



(Figure 1)



(Figure 2)

References

[1] L. Rapp, J. Ailuno, A.-P. Alloncle, Ph. Delaporte, 'Pulsed-laser printing of silver nanoparticles ink: control of morphological properties', Optics Express **19** (22), 21563–21574, (2011)

[2] J. Wang, R. C. Y. Auyeung, H. Kim, N. A. Charipar, A. Piqué, 'Three-Dimensional Printing of Interconnects by Laser Direct-Write of Silver Nanopastes', Adv. Mater. **22**, 4462–4466, (2010)

[3] L. Rapp, E. Biver, A. P. Alloncle, Ph. Delaporte, 'High-Speed Laser Printing of Silver Nanoparticles Ink', J. of Laser Micro/NanoEnginnering **9** (1), 5-9, (2014)

[4] Ch. Boutopoulos, I. Kalpyris, E. Serpetzoglou, I. Zergioti, Laser-induced forward transfer of silver nanoparticle ink: time-resolved imaging of the jetting dynamics and correlation with the printing quality, Microfluid Nanofluid **16**(3), 493-500, (2014)

[5] E. Biver, L. Rapp, A. P. Alloncle, P. Serra, Ph. Delaporte, 'High-Speed Multi-Jets Printing using Laser Forward Transfer: Time-Resolved Study of the Ejection Dynamics', Optics Express **22** (14), 17122–17134, (2014)

[6] A. Patrascioiu, C. Florian, J.M. Fernández-Pradas, J.L. Morenza, G. Hennig, P. Delaporte, P. Serra, 'Interaction between jets during laser-induced forward transfer', Applied Physics Letters **105**, 014101 (2014)

Biography

Philippe Delaporte is Director of Research at CNRS. He obtained the Engineer Diploma (1984) and Ph.D. degree (1987) at Aix-Marseille University. Since 1988, he has been staff member scientist at the LP3 laboratory. Since 2012, he is the director of the LP3 laboratory (CNRS - Aix-Marseille University). In 1992, he obtained the bronze medal of the French National Centre of Scientific Research (CNRS) for his work on ionic excimers. He is also vice-president of the photonic cluster 'OPTITEC'. His research directions are now focused on laser ablation and the development of pulsed laser applications such as laser printing and surface structuring. He is author or co-author of more than 130 articles in peer-review journals, 4 chapters of books as well as more than 100 papers in proceedings of international conferences. He gave 70 invited presentations in international conferences. He was the coordinator of the FP7 collaborative project e-LIFT (2010-2012).

(P.31) Digital Laser Thin Film Layer Patterning of Transistor Electrodes on Flexible Substrate

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Abstract

Photolithography, due to its high resolution and good edge control, is the preferred technology for transistor patterning on embedded circuit. However, the high costs of photolithographic manufacturing processes including the design and production of several projection masks make this manufacturing method suitable mostly for high volume production. This can become a severe constraint for rapid prototyping and low-medium volume production.

Laser ablation is a direct writing technique which when combined with CNC or optical axes becomes fully digital. This combination unlocks unlimited prototyping potential with design flexibility of the surface pattern at almost no additional costs or lead time. Laser ablation is also selective, since the correct choice of laser wavelength, pulse duration and incident power restricts the damage area affected by the radiation. This is especially useful when the target under process is a stack of superposed thin film layers.

Direct laser ablation can be used as an alternative cost-effective, mask-less technique with respect to traditional photolithography, maintaining at the same time sufficient feature quality, edge control and position accuracy as delivered by traditional photolithographic techniques.

In this work we take the manufacturing of flexible display backplanes as case study to obtain an industrially robust and fully digital process for low-medium volume patterning of organic transistor (OTFT) electrodes. To explore the effects of laser wavelength and pulse duration, ultrafast diode-pumped solid state (DPSS) lasers at different wavelengths have been used. Excellent results have been obtained realising fully working OTFT stacks with attractive electrical performance as compared to the standard OTFT transistor performance obtained by photolithography.

This work is funded by "Innovate UK", grant agreement 44069-315222, project SCULPT

Biography

Mr. Riccardo Geremia received his Bachelor and Master of Science Degrees in Physics Engineering at Politecnico di Milano (Milan, Italy). From 2012 to 2013 he collaborated with Dr. Osellame's research group for the prototyping of integrated optical devices made by femtosecond lasers in the field of Quantum Information. In 2013 he worked for Optotec s.p.a (Garbagnate Milanese, Italy) on the design, fabrication and packaging of integrated optical circuits. At the beginning of 2014 he joined the R&D department of Oxford Lasers, where he is currently working on the development of new micromachining processes and products. In September 2015 he started an Engineering Doctorate program at Heriot-Watt University (Edinburgh).

(P.32) Laser processing for P3-scribing on CIGS based solar cell

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Abstract

CIGS thin film solar cells are very attractive for energy production due to their potential of high performance, low production cost and flexible ability. The patterning of the panel in several cells is an essential process to ensure optimized performances on large area panels. Laser scribing of thin film solar cell is a promising approach that permits non-contact and fast process suitable for industrial production.

In our study, ultra-short lasers (femtosecond and picosecond pulse duration) emitting at 515 nm are used to perform the ablation of the TCO (Transparent Conductive Oxyde) plus CIGS thin film stack while keeping intact the Molybdenum underlayer. This permits the achievement of the so-called P3 scribing for cell isolation. A scanner system coupled to F-theta lens is used for fast beam motion required for using high repetition rate laser conditions (up to 200 kHz). We optimized the laser irradiation parameters to preserve the electrical cell performances after the scribing step with both picosecond and femtosecond pulse duration. First, we find that laser energy has to be reduced near the ablation threshold in order to minimize heating of the CIGS layer at the borders of the ablated zone. This can be responsible for local changes in CIGS properties causing high leakage current and reducing the cell performances. Second, we highlight the interest of using femtosecond laser when working with high repetition rate conditions. We also investigate the possibility to remove only the TCO layer to perform the P3 scribing on module.

Our study highlights that laser ablation allows better precision and morphological quality for P3 scribing of CIGS-based solar cell compared to mechanical tip process. This makes laser scribing process an interesting tool to decrease the dead area of the panels and then increase the module performances.

Keywords: CIGS solar cell, laser processing, P3 laser scribing, thin film laser ablation.

Biography

Stéphanie Leyder obtained her PhD in 2013 at the LP3 laboratory on the nonlinear interaction inside dielectric and semiconductor materials using infrared femtosecond laser. Then, she moved to Oxford Lasers Company, in the frame of the European project 'LaserMicroFab', to develop laser process for organic thin film material. She is now working on the laser ablation of CIGS thin film solar cell in a collaborative project between industry and academic partners.

(P.33) Fault-tolerant strategies for printed electronics

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Abstract

This paper focuses on fault-tolerant design strategies for printable electronics with an emphasis on future industrial and high-reliability applications, for which the printed circuit must be robust in the presence of various fault mechanisms. Significant progress towards has been made towards rapid manufacturing of printed devices, including large area 3D printing that competes with established optical lithography systems [1], additive printing with integrated conductive track deposition [2] and even self-healing interconnects [3]. However, applications for printed electronics are mostly aimed at consumer devices rather than high value industrial system and sub-systems where high-reliability service-driven considerations are most prevalent [4]. While material and deposition techniques for printed electronics are advancing at a significant rate, there remains a strong need for design toolkits to assist with design optimisation and prediction of application-specific reliability [5].

There is a renewed interest in functional design hardening for traditional silicon circuits and future nanoscale electronics, driven primarily by their increasing susceptibility to random single event upset (SET) and accelerated degradation in harsh environments that is exacerbated by aggressive technology scaling (threshold voltage, transistor scaling and power density). This is particularly acute in state-of-the-art electronic sub-systems that utilise high-density system-on-chip (SoC) chips and 3D additive printing as found in the emerging autonomous vehicles, avionics and space sectors [6–9]. Similar challenges will face printed electronics with respect to fault mechanisms such as high temperature operation, interconnect and packaging integrity for flexible devices and stability of device characteristics, all of which influence the overall device failure rate.

The work presented here seeks to address the above concerns by adopting a fault tolerant design strategy at the transistor level that addresses stuck-at fault conditions caused by transistor or interconnect failure. Self-healing concepts are considered, including self-detection, self-repair and self-isolation [10,11] and the proposed strategy assists in the detection and classification of fault events via built in fault signals triggered by specific faults. A semi-analogue condition is exploited within CMOS or pseudo-CMOS gates that enables fault discrimination and automatic masking of sub-critical faults [12] with a 2x overhead of transistors. The method is well-suited to medium and high density logic designs with built-in fault detection buses that enable close monitoring of the printed circuit status and potentially triggers additional active fault mitigation strategies.

Detailed fault behaviour is analysed theoretically and confirmed experimentally via fault injection test bench. Following this, considerations for integrating the design strategy into functional logic units are discussed. Finally, future work is identified including modelling the semi-analogue behaviour of CMOS/p-MOS printed FETS via design SPICE models and their fault monitoring as well as the protection of larger printed FETs devices for power circuitry.

References

1. D. Radtke and U. D. Zeitner, "Laser-lithography on non-planar surfaces," Opt. Express **15**, 1167 (2007).
2. S. Molesa, D. R. Redinger, D. C. Huang, and V. Subramanian, "High-quality inkjet-printed multilevel interconnects and inductive components on plastic for ultra-low-cost RFID applications," in *Symposium H – Flexible Electronics - Materials and Device Technology*, MRS Online Proceedings Library Archive (2003), Vol. 769.
3. S. R. Baliga, M. Ren, and M. N. Kozicki, "Self-healing interconnects for flexible electronics applications," Thin Solid Films **519**, 2339–2343 (2011).
4. D. C. Brauer and G. D. Brauer, "Reliability-Centered Maintenance," IEEE Trans. Reliab. **R-36**, 17–24 (1987).
5. "TDK4PE Technology & Design kit for printed electronics," http://www.tdk4pe.eu/.
6. "Space Station's 3D Printer Makes 1st Part," http://www.space.com/27861-3d-printer-space-station-first-part.html.
7. "AirbusVoice: How 3D Printing Is Delivering Airplane Parts On Demand - Forbes," http://www.forbes.com/sites/airbus/2014/07/15/how-adding-a-new-dimension-to-airplanes-is-delivering-parts-on-demand/.
8. "3D opportunity for the Department of Defense: Additive manufacturing fires up - Deloitte University Press," http://dupress.com/articles/additive-manufacturing-defense-3d-printing/.
9. R. R. Tummala, "SOP: what is it and why? A new microsystem-integration technology paradigm-Moore's law for system integration of miniaturized convergent systems of the next decade," IEEE Trans. Adv. Packag. **27**, 241–249 (2004).
10. R. Frei, R. McWilliam, B. Derrick, A. Purvis, A. Tiwari, and G. D. M. Serugendo, "Self-healing and self-repairing technologies," Int. J. Adv. Manuf. Technol. **69**, 1033–1061 (2013).
11. J. Schumann, O. J. Mengshoel, and T. Mbaya, "Integrated Software and Sensor Health Management for Small Spacecraft," in *Proc. of IEEE International Conference on Space Mission Challenges for Information Technology* (2011), pp. 77–84.
12. R. McWilliam, P. Schiefer, and A. Purvis, "Experimental Validation of a Resilient Electronic Logic Design with Autonomous Fault Discrimination/Masking," Procedia CIRP **38**, 265–270 (2015).

(P.34) Regioregular synthesis of accetor-functionalised oligothiophenes.[1]

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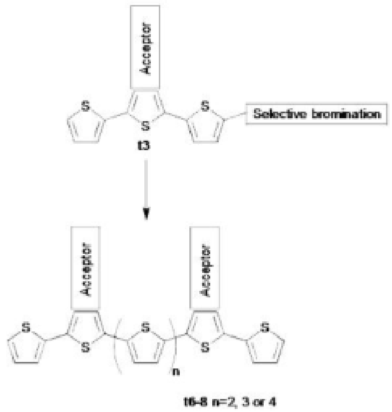
Abstract
Acceptor-functionalised short-chain linear oligothiophenes have received considerable attention over recent years, and have been utilized in organic photovoltaic (OPV) cells, organic field effect transistors (OFETs), and organic light emitting diodes (OLEDs).

The synthesis of acceptor-functionalised oligothiophene derivatives (**t3**, **t6**, **t7**, **t8**) is described, where the acceptor units are arranged in a head-to-head regioregular-like motif. This head-to-head dimerisation stems from the ability to selectively brominate the conjugated thiophene moiety of the unsymmetrical building block **t3** from an intramolecular charge-transfer polarisation. Compounds **t3** to **t8** show a significant increase in absorption in the near-infrared region and a decrease in the HOMO energy occurs, which may promote their future application as optoelectronic materials.



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(P.35) Roll to Roll Patterning of Thin Film Transistor Contacts

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Abstract
Patterning was identified by the OE-A 2015 6th edition roadmap as a key challenge for flexible technology. Combining precision patterning with high throughput systems like roll-to-roll is therefore also key for large area electronics be it photovoltaics or electronic circuitry. Flexography is a roller based printing system which has already been used to pattern organic and inorganic layers of transistors. This research has demonstrated that patterned electrodes can be created using flexography in a vacuum roll-to-roll system. This has been complimented by the use of silicone soft stamp lithography to investigate resolution limits of this patterning technique.

(P.36) Large volume continuous synthesis of metal oxide nanoparticle inks toward inkjet printed TFT devices

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Abstract
In contrast to lab-scale approaches, industrial manufacturing requires large-volume, inexpensive, and well-controllable processes. Mixed metal oxide nanoparticle based thin films offer a wide range of functionalities and electrical properties tuneable by composition.

An ink for solution processed semiconducting thin films is developed based on a continuous solvothermal synthesis process. IZO nanoparticles inks with an average size of 50 nm showing intrinsic stabilization in a mixed polyol / alcohol solvent have been produced, which are further modified for spin and inkjet processing.

Bottom-gate top-contact thin-film transistors (TFTs) were fabricated by spin coating and inkjet printing on to a p_{+}- Si/SiO_2 substrate. S / D electrodes were either inkjet printed with a conductive silver ink or evaporated aluminium.

Annealing of the semiconducting layer in air yields TFT devices with an ON/OFF ratio between $1x10^5$ and $1x10^6$ and a saturation mobility of 0.6 cm^2/Vs. Due to the unpatterned semiconductor layer, the observed gate leakage is only two orders of magnitude below the ON current ($1x10^{-5}$ A). Inkjet printed TFTs show a gate leakage reduction of four decades and an ON / OFF ratio between $1x10^6$ and $1x10^7$ at a reduced saturation mobility of 0.014 cm^2/Vs ($V_d = 40$ V).

The controlled and continuous production of metal oxide nanoparticles delivers a versatile and facile basis for industrial-scale solution processing of inorganic semiconductors. The presented approach yields performance values close to amorphous silicon and has a high potential for further improvements.

Biography

Dr Sean Butterworth: Sean joined Promethean as a Research Scientist in 2013 upon completion of his PhD in polymer and colloid science at the University of Manchester and now holds a Senior Scientist position at Promethean. Sean has extensive experience in materials research for printed electronics applications and ink formulation.

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